Delta-Sigma Modulators with Low Oversampling Ratios

by

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ABSTRACT

This dissertation explores methods of reducing the *oversampling ratio* (OSR) of both *delta-sigma* ($\Delta\Sigma$) modulators and incremental data converters. The first reduced-OSR architecture is the high-order cascaded $\Delta\Sigma$ modulator. These $\Delta\Sigma$ modulators are shown to reduce the in-band noise sufficiently at OSRs as low as 3 while providing power savings. The second low OSR architecture is the high-order cascaded incremental data converter which possesses *signal-to-quantization noise ratio* (SQNR) advantages over equivalent $\Delta\Sigma$ modulators at low OSRs. The final architecture is the time-interleaved incremental data converter where two designs are identified as potential methods of increasing the throughput of low OSR incremental data converters. A prototype chip is designed in 0.18 µm CMOS technology which can operate in three modes by simply changing the resetting clock phases. It can operate as an 8-stage pipeline *analog-to-digital* (A/D) converter, an 8^{th}-order cascaded $\Delta\Sigma$ modulator, and an 8^{th}-order cascaded incremental data converter with an OSR of 3.

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Finally, I would not have accomplished anything without the support of my family. I thank my brother Daryl, my sister Lauren, and especially my parents Douglas and Cheryl for everything they have done to get me this far in my education. Most importantly I thank my girlfriend Paula who has been at my side for the entire degree, through the dizzying highs, the terrifying lows, and everything in between.

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List of Abbreviations

ADSL ..... Asymmetric Digital Subscriber Line
A/D ..... Analog-to-Digital
CMFB ..... Common-Mode Feedback
CMOS ..... Complementary Metal-Oxide-Semiconductor
CMRR ..... Common-Mode Rejection Ratio
CQFP ..... Ceramic Quad Flat Pack
DNL ..... Differential Non-Linearity
D/A ..... Digital-to-Analog
ENOB ..... Effective Number of Bits
FFT ..... Fast Fourier Transform
FR-4 ..... Flame Retardant 4
INL ..... Integral Non-Linearity
LSB ..... Least Significant Bit
MASH ..... Multi-Stage Noise-Shaping
MSB ..... Most Significant Bit
NMOS ..... N-channel Metal-Oxide-Semiconductor
NTF ..... Noise Transfer Function
OSR ..... Oversampling Ratio
OTA ..... Operational Transconductance Amplifier
PCB ..... Printed Circuit Board
PMOS ..... P-channel Metal-Oxide-Semiconductor
PSD ..... Power Spectral Density
SFDR ..... Spurious-Free Dynamic Range
SNDR ..... Signal-to-Noise and Distortion Ratio
SNR ..... Signal-to-Noise Ratio
SQNR ..... Signal-to-Quantization Noise Ratio
STF ..... Signal Transfer Function
S/H ..... Sample-and-Hold

Chapter 1

Introduction

DELTA-SIGMA ($\Delta\Sigma$) modulation efficiently performs high resolution data conversion using oversampling. With increasing bandwidth demands, reducing the *oversampling ratio* (OSR) is important to meet the required input bandwidth while also attaining medium to high resolution as expected from oversampled converters. The purpose of this research is to investigate the effect of reducing the OSR of $\Delta\Sigma$ modulators and incremental data converters.

1.1 Motivation

High-speed data converters operating on input signal bandwidths in the megahertz range are key analog building blocks for a variety of applications including high-speed wireless and wireline communication systems, high-quality video systems, imaging systems, and instrumentation systems. A few examples include lower-bandwidth applications such as *asymmetric digital subscriber line* (ADSL) which require 14 bit resolution with a 2.2 MHz signal bandwidth [1], higher speed television receivers which require a bandwidth of 8 MHz per channel but only 9 bit resolution [2], or high-speed video decoding which requires data conversion at sampling frequencies as high as 150 MHz at 10 bit resolution [3].

When higher accuracy but lower bandwidth is needed, oversampling techniques are typically employed. High OSRs are desirable since the requirements on the individual circuits are relaxed based on the OSR. However, increased bandwidth requirements necessitate techniques to reduce the OSR while still attaining good performance. The most common

oversampled data converter is the ΔΣ modulator which efficiently performs high-resolution data conversion and is typically reserved for high OSR applications where noise-shaping increases the *signal-to-quantization noise ratio* (SQNR). The difficulty at low OSRs is that noise-shaping is not as efficient because it increases the total noise power in the system thereby reducing the SQNR. Oversampled cascaded or *multi-stage noise-shaping* (MASH) architectures provide an alternative as they are more stable than single-stage architectures [4], but are more sensitive to non-idealities in the circuit.

Nyquist-rate *analog-to-digital* (A/D) converters can be used at low OSRs [5], and they typically require some oversampling to reduce the requirements on the anti-aliasing filter at the input. However, they lose a significant advantage provided by noise-shaping since input-referred noise gets shaped by gain stages rather than the integrators present in noise-shaping converters. This is a fundamental disadvantage of pipeline A/D converters when compared to ΔΣ modulators.

1.2 Current Literature

1.2.1 High-Speed ΔΣ Modulators

In the last several years there has been considerable research on high-speed ΔΣ modulators with OSRs of 16 or less. Table 1.1 summarizes some experimental results in *complementary metal-oxide-semiconductor* (CMOS) technology for recently published high-speed ΔΣ modulators with OSRs of 16 or less.

The modulators with the highest sampling frequencies are continuous-time. This is expected since the maximum sampling frequency of continuous-time modulators is dependent on the feedback path which includes the quantizer regeneration time and the feedback *digital-to-analog* (D/A) converter, while discrete-time modulators depend on the *operational transconductance amplifier* (OTA) settling [4]. Despite their inferior speed, discrete-time modulators are still shown to operate at sampling frequencies of 100 MHz or more.

The lowest reported OSR for a cascaded architecture is 4 [11, 14]. To the author's knowledge, no implementation of a cascaded ΔΣ modulator exists with a lower OSR. In this dissertation a 10-bit 8-stage cascaded ΔΣ architecture with an OSR of 3 is proposed, as well as an 11-bit 8-stage cascaded incremental A/D converter. Both the low OSR and high number of cascaded stages have never been implemented before.

Ref.	Technology	Architecture	Sampling Frequency	Signal Bandwidth	OSR	SNDR	Power
[6]	0.25 µm	5^{th}-order (C)	60 MHz	2.5 MHz	12	80 dB	50 mW
[7]	0.18 µm	0-3 MASH (D)	50 MHz	3.1 MHz	8	64 dB	22 mW
[8]	90 nm	4^{th}-order (D)	100 MHz	4 MHz	12.5	67 dB	12 mW
[9]	0.18 µm	2^{nd}-order TI (D)	100 MHz	4.2 MHz	12	79 dB	28 mW
[10]	0.18 µm	2-1 MASH (C/D)	240 MHz	7.5 MHz	16	67 dB	89 mW
[11]	0.13 µm	1-2 MASH (D)	80 MHz	10 MHz	4	50 dB	60 mW
[12]	0.18 µm	3^{rd}-order TI (C)	100 MHz	10 MHz	5	57 dB	101 mW
[13]	0.18 µm	2-2 MASH (C)	160 MHz	10 MHz	8	57 dB	122 mW
[14]	0.18 µm	2-0 MASH (D)	80 MHz	10 MHz	4	73 dB	240 mW
[15]	0.25 µm	2^{nd}-order (C)	320 MHz	10 MHz	16	54 dB	15 mW
[16]	0.18 µm	4^{th}-order (C)	276 MHz	11.5 MHz	12	69 dB	21 mW
[17]	0.18 µm	5^{th}-order (D)	200 MHz	12.5 MHz	8	72 dB	200 mW
[18]	0.13 µm	4^{th}-order (C)	300 MHz	15 MHz	10	64 dB	70 mW
[12]	0.18 µm	3^{rd}-order TI (C)	200 MHz	20 MHz	5	49 dB	103 mW
[11]	0.13 µm	1-2 MASH (D)	160 MHz	20 MHz	4	50 dB	87 mW
[19]	0.13 µm	3^{rd}-order (C)	640 MHz	20 MHz	16	74 dB	58 mW

Table 1.1: Recently published experimental results for high-speed continuous-time (C) and discrete-time (D) ΔΣ modulators at low OSRs in CMOS technology, in order of increasing signal bandwidth.

1.2.2 High-Speed Pipeline A/D Converters

Current research in high-speed pipeline A/D converters shows that in CMOS technology only a few implementations exist with sampling frequencies greater than 200 MHz, and those data converters have resolutions less than 9 bits, where resolution refers to *signal-to-noise and distortion ratio* (SNDR). Table 1.2 summarizes these recent experimental results.

The results of Table 1.2 are a good indicator of the maximum sampling frequency for discrete-time ΔΣ modulators. Pipeline A/D converters have slightly higher maximum sampling frequencies than discrete-time ΔΣ modulators, but it will be shown that the design of cascaded ΔΣ modulators at low OSRs is similar to the design of pipeline A/D converters,

Ref.	Technology	Sampling Frequency	Signal Bandwidth	SNDR	Power
[20]	0.18 µm	100 MHz	50 MHz	54 dB	67 mW
[21]	0.18 µm	100 MHz	50 MHz	55 dB	33 mW
[22]	0.18 µm	100 MHz	50 MHz	72 dB	230 mW
[23]	90 nm	100 MHz	50 MHz	73 dB	250 mW
[24]	90 nm	100 MHz	50 MHz	70 dB	130 mW
[25]	0.18 µm	110 MHz	55 MHz	64 dB	97 mW
[26]	0.18 µm	125 MHz	62.5 MHz	53 dB	40 mW
[27]	0.18 µm	125 MHz	62.5 MHz	69 dB	909 mW
[28]	0.18 µm	125 MHz	62.5 MHz	78 dB	385 mW
[29]	0.18 µm	150 MHz	75 MHz	52 dB	123 mW
[30]	0.25 µm	180 MHz	90 MHz	63 dB	756 mW
[31]	0.18 µm	200 MHz	100 MHz	48 dB	30 mW
[32]	0.13 µm	200 MHz	100 MHz	52 dB	104 mW
[33]	90 nm	200 MHz	100 MHz	54 dB	55 mW
[34]	90 nm	200 MHz	100 MHz	62 dB	348 mW
[27]	90 nm	205 MHz	102.5 MHz	54 dB	61 mW
[35]	0.13 µm	220 MHz	110 MHz	54 dB	135 mW
[36]	0.13 µm	250 MHz(x4)	125 MHz(x4)	55 dB	250 mW
[37]	0.13 µm	400 MHz	200 MHz	54 dB	160 mW
[38]	90 nm	500 MHz	250 MHz	53 dB	55 mW

Table 1.2: Recently published experimental results for high-speed pipeline A/D converters in CMOS technology.

and for that reason $\Delta\Sigma$ modulators should attain equally fast sampling frequencies.

1.3 Outline

The dissertation is organized as follows: Chapter 2 provides some background information on the various A/D converter architectures necessary for understanding the material pre-

sented. Chapter 3 discusses the operation of $\Delta\Sigma$ modulators at low OSRs while Chapter 4 presents the operation of incremental A/D converters at low OSRs. The design of a prototype chip fabricated in 0.18 µm CMOS technology is described in Chapter 5, and Chapter 6 presents the experimental results from the prototype in its three modes of operation as a pipeline A/D converter, a $\Delta\Sigma$ modulator and an incremental A/D converter. Chapter 7 concludes the dissertation. Derivations of the incremental A/D converter resolution and the DC gain requirements of the incremental A/D converter are given in Appendix A and Appendix B, respectively. An alternative implementation to the time-interleaved incremental data converter architecture presented in Chapter 4 is given in Appendix C.

Chapter 2

Background Information

The basic operation of various data converters, including ΔΣ modulators, incremental A/D converters, pipeline A/D converters and time-interleaved A/D converters are explained in this chapter. The fundamental trade-offs between power, resolution and bandwidth are also discussed.

2.1 ΔΣ Modulators

ΔΣ modulators employ both oversampling and noise-shaping to improve the accuracy of a low-resolution (as low as 1-bit) internal A/D converter, or quantizer. With the feedback loop the noise in the quantizer has a different transfer function to the output than the signal. This allows the designer to choose a filter that will shape the noise and keep it small in the band of interest (which is dependent on the OSR), while also keeping the signal unattenuated in this frequency range.

As shown in Fig. 2.1, only a small portion of the frequency band is kept through digital filtering leaving little noise within the band of interest, resulting in a high-resolution A/D converter at a reduced speed. The *noise transfer function* (NTF) and the *signal transfer function* (STF) characterize the ΔΣ modulator. Referring to Fig. 2.2 (assuming an internal A/D and D/A reference voltage V_{REF} with $D_1 \in [-1,1]$), the NTF is

$$\frac{D_{OUT} \cdot V_{REF}}{E_1} = \frac{1}{1 - L_1(z)} \tag{2.1}$$

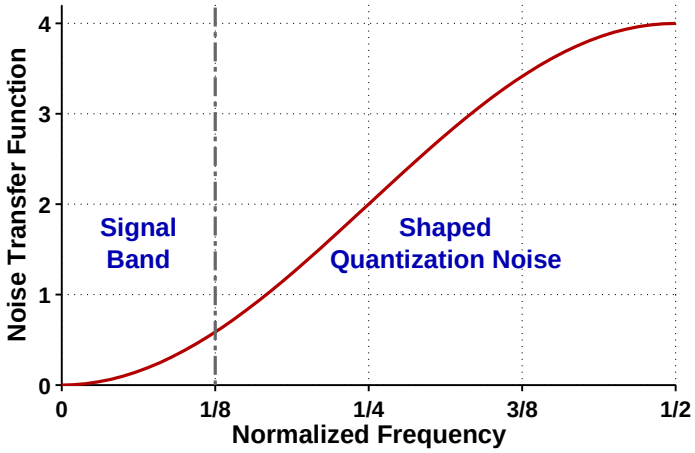


Figure 2.1: Spectral operation of a ΔΣ modulator.

while the STF is

$$\frac{D_{OUT} \cdot V_{REF}}{V_{IN}} = \frac{L_0(z)}{1 - L_1(z)}. \tag{2.2}$$

The order and shape of the transfer functions, the OSR, and the internal A/D converter resolution determine the resolution of the ΔΣ modulator.

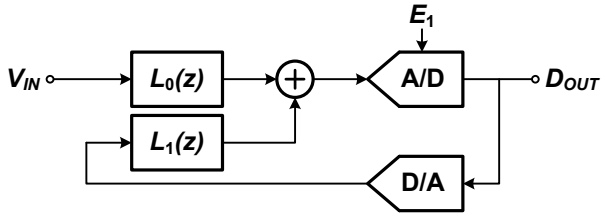


Figure 2.2: General architecture of a ΔΣ modulator characterized by the two loop filters $L_0(z)$ and $L_1(z)$ (without the decimation filter).

2.1.1 Single-Stage ΔΣ Modulators

A generalized single-stage modulator was shown in Fig. 2.2. They are characterized by a single quantizer, NTF and STF. High resolution ΔΣ modulators are designed with high OSRs, high-order NTFs, and multi-bit quantizers [4]. For high-bandwidth applications the OSR must be reduced, leaving only the NTF and quantizer resolution as a design parameter for increased resolution.

One significant improvement in ΔΣ modulators is the use of an input feed-forward path [39]. An extra feed-forward branch is added from the input to the summer in front of the quantizer. With this architecture, the NTF remains unchanged, but the STF is

$$\frac{D_{OUT} \cdot V_{REF}}{V_{IN}} = \frac{1 + L_0(z)}{1 - L_1(z)}. \tag{2.3}$$

For the input feed-forward architecture, if $L_0(z) = -L_1(z)$ the STF becomes unity. This modifies the general structure of Fig. 2.2 to that shown in Fig. 2.3. More important than the unity-gain STF, the signal content at the loop filter output is minimized. Shown in Fig. 2.3, the delay-free path from the input through the A/D and D/A comes back and subtracts from the input. No signal content enters the loop filter, and all that is left is the error signal E_1. Therefore, the loop filter output is only a function of E_1. E_1 will always be somewhat correlated with the input, but for a higher-resolution internal A/D converter the input will be less correlated, and distortion introduced by the loop filter will be less signal dependent. This is advantageous as low-distortion OTAs become more difficult to design with increasingly smaller power supplies [40, 41].

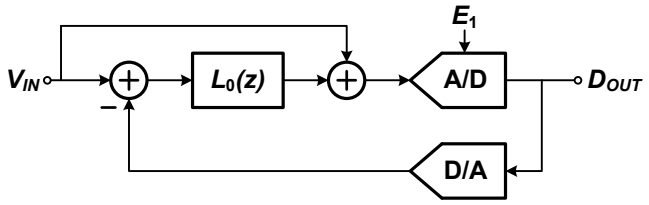


Figure 2.3: Input feed-forward architecture for a general ΔΣ modulator (without the decimation filter).

2.1.2 Cascaded ΔΣ Modulators

For stability reasons, it is difficult to design a high-order NTF and keep it stable as the filter coefficients vary, or the loop becomes nonlinear. There is also a trade-off between the NTF stability and how aggressively it shapes the noise (i.e., how much resolution it obtains). For these reasons high-resolution or low OSR ΔΣ modulators are often implemented with cascaded architectures.

As the name implies, cascaded (or MASH) ΔΣ modulators cascade two or more single-stage ΔΣ modulators. They are named based on the order of each stage; a 2-1 MASH ΔΣ

cascades a 2nd-order ΔΣ with a 1st-order ΔΣ. An $L-0$ Leslie-Singh architecture [42], or $0-L$ architecture [43] refers to an L^{th}-order ΔΣ followed or proceeded by a Nyquist-rate A/D converter, where the Nyquist-rate converter is loosely considered a 0^{th}-order ΔΣ.

A general two-stage cascaded ΔΣ modulator is shown in Fig. 2.4. The advantage of cascaded modulators is that no individual modulator needs to be designed with a high-order filter; the total filter order can be spread out across many different stages so that each individual ΔΣ stage will only be of lower order (1st-order, 2nd-order, or maybe 3rd-order). The modulator stability will be a function of the individual lower order modulators rather than the total order of the modulator.

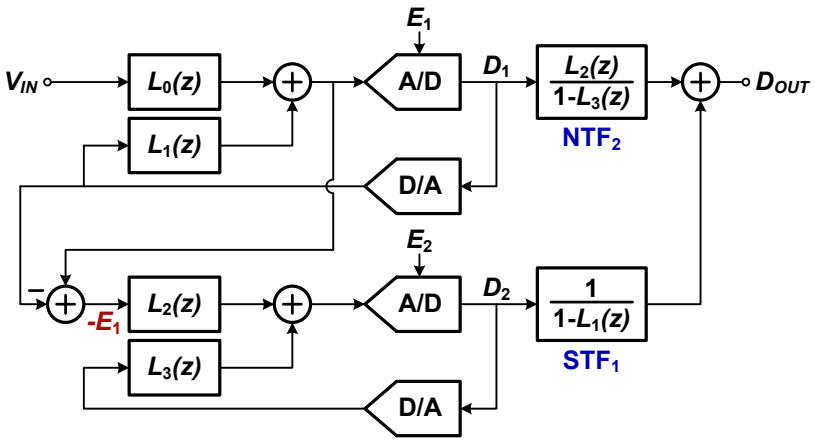


Figure 2.4: General 2-stage cascaded ΔΣ modulator where loop filters $L_0(z)$ and $L_1(z)$ characterize the first stage, and $L_2(z)$ and $L_3(z)$ characterize the second stage.

A digital filter is required to recombine the digital outputs of the individual ΔΣ modulators. It is designed to cancel the error introduced in the first stages, leaving only the error introduced in the last of the cascaded stages which will be noise-shaped by the product of the NTF of each stage. This cancelation is dependent on matching between the digital filters and the analog filters within the individual ΔΣ modulators; this is one of the major limitations for high-resolution cascaded ΔΣ modulators [44].

As shown in Fig. 2.4, when the error signal -E_1 is passed to the next stage, the output of each of the individual modulators are

$$D_1 \cdot V_{REF} = V_{IN}\frac{L_0(z)}{1-L_1(z)} + E_1\frac{1}{1-L_1(z)} \tag{2.4}$$

and

$$D_2 \cdot V_{REF} = -E_1 \frac{L_2(z)}{1-L_3(z)} + E_2 \frac{1}{1-L_3(z)}. \tag{2.5}$$

In order to cancel the error signal E_1, $D_1 \cdot V_{REF}$ is multiplied by the second stage NTF, and D_2 is multiplied by the first stage STF. The resulting output is

$$\begin{aligned} D_{OUT} \cdot V_{REF} &= D_1 \cdot V_{REF} \frac{L_2(z)}{1-L_3(z)} + D_2 \cdot V_{REF} \frac{1}{1-L_1(z)} \\ &= V_{IN} \frac{L_0(z)}{1-L_1(z)} \frac{L_2(z)}{1-L_3(z)} + E_2 \frac{1}{1-L_1(z)} \frac{1}{1-L_3(z)} \\ &= V_{IN} \cdot \mathrm{STF}_1 \cdot \mathrm{STF}_2 + E_2 \cdot \mathrm{NTF}_1 \cdot \mathrm{NTF}_2. \end{aligned} \tag{2.6}$$

It is clear that D_{OUT} is no longer a function of E_1, and the overall NTF on the error signal E_2 is the cascaded NTF of both individual stages (NTF_1 and NTF_2), while the overall STF on the input signal V_{IN} is the cascaded STF of both individual stages (STF_1 and STF_2).

As mentioned above, when the input feed-forward architecture is used, the loop filter output contains no signal component. Depending on the quantizer resolution, this error signal might be considerably smaller than the input range of a ΔΣ modulator. When the error signal is passed to the subsequent stage, it may be possible to amplify it while staying within the allowable input range. The amplification factor will increase the overall resolution of the cascaded ΔΣ by the same amount.

With the input feed-forward architecture, the loop filter can be manipulated so that the integrator output is a delayed version of the error signal. An example of this in a 2-1 cascaded ΔΣ modulator is shown in Fig. 2.5. The first stage has an NTF of $(1-z^{-1})^2$ while the second stage has an NTF of $(1-z^{-1})$. The second integrator output in the first stage is the inverted error signal from the first quantizer -E_1, delayed by two samples. Assuming it is small enough (equivalently, the quantizer resolution is high enough), it can be multiplied by an interstage gain factor G. After the digital cancellation filter, the final output is

$$D_{OUT} \cdot V_{REF} = z^{-3} V_{IN} + \frac{(1-z^{-1})^3}{G} E_2. \tag{2.7}$$

The overall NTF is $(1-z^{-1})^3/G$, the expected 3$^{\mathrm{rd}}$-order NTF $(1-z^{-1})^3$ reduced by the interstage gain factor G. The STF is simply the input V_{IN} delayed by three samples. Since the second stage output is a delayed version of its error signal E_2, this could easily be passed

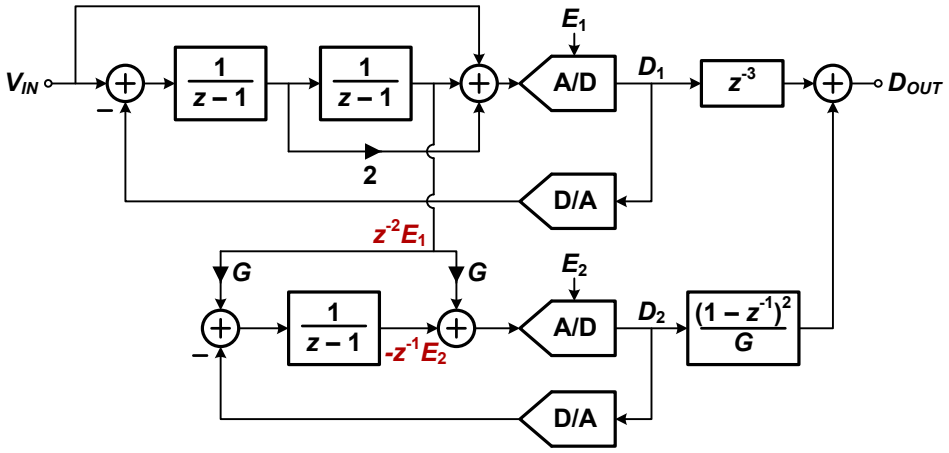


Figure 2.5: Input feed-forward 2-1 cascaded ΔΣ modulator. The interstage gain G improves the resolution by G.

on to a third stage with additional cascading.

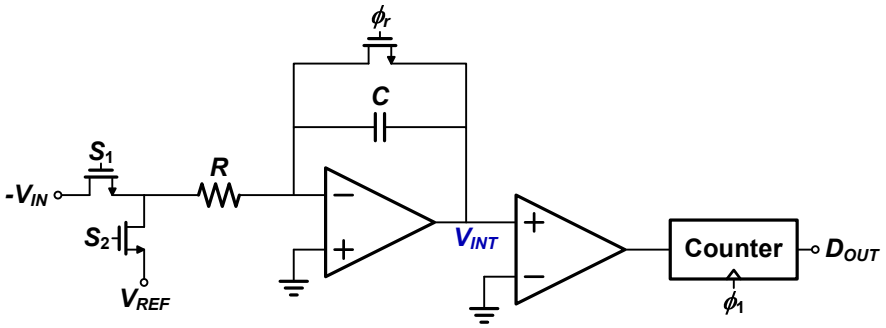
2.2 Incremental Data Converters

Incremental A/D converters are best understood as a combination of ΔΣ modulators and dual-slope A/D converters. They act like dual-slope A/D converters mixed in time, but also have the benefit of utilizing higher-order loop filters like ΔΣ modulators.

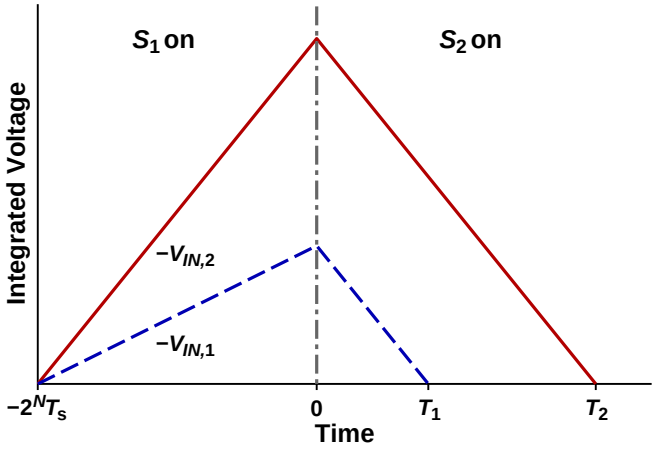
2.2.1 Dual-Slope A/D Converters

The dual-slope (or integrating) A/D converter is useful for high-accuracy, high-linearity conversion with low offset and gain errors [45]. Shown in Fig. 2.6, the converter integrates the input signal for a fixed time and then subtracts a reference voltage for a counted number of clock periods until the output crosses zero. The final count at the zero crossing is the resulting digital output. For an N-bit A/D converter, 2^{N+1} cycles are required for one conversion. For high-resolution A/D converters the conversion time can severely limit the speed at which they operate.

During the first phase when S_1 is on, the input -V_{IN} is integrated. After 2^N clock cycles



(a) Architecture



(b) Time-Domain Integrator Output

Figure 2.6: Dual-slope A/D converter. The input signal is integrated on S_1 while the reference voltage is integrated and subtracted from the input on S_2. ϕ_1 is operating at the sampling frequency f_s. T_1 and T_2 are proportional to their respective digital outputs.

(the entire S_1 phase), the integrator output will be

$$V_{INT} = -\int_{-2^N T_s}^{0} \frac{-V_{IN}}{RC} d\tau = \frac{V_{IN}}{RC} \cdot 2^N T_s. \tag{2.8}$$

On the second phase, S_1 is off and S_2 is on. V_{REF} is then integrated until the voltage at V_{INT} goes to zero. The voltage at the integrator output during S_2 is

$$V_{INT} = -\int_{0}^{t} \frac{V_{REF}}{RC} dt + \frac{V_{IN}}{RC} \cdot 2^N T_s. \tag{2.9}$$

After t seconds, the voltage is

$$V_{INT} = \frac{V_{IN} \cdot 2^N T_s - V_{REF} \cdot t}{RC}. \tag{2.10}$$

This voltage is zero when

$$t_0 = \frac{V_{IN}}{V_{REF}} \cdot 2^N T_s. \tag{2.11}$$

It is clear from this equation that the time t_O when V_{INT} crosses zero is proportional to the ratio of V_{IN}/V_{REF} discretized in steps of T_s, where T_s is the time-domain *least significant bit* (LSB) of the N-bit output.

If V_{IN} has a frequency dependent component ($V_{IN,\sim}$) along with a constant input ($V_{IN,-}$), then the output of the first integration phase is

$$\begin{aligned} V_{INT} &= \int_{-2^N T_s}^{0} \frac{V_{IN}}{RC} d\tau \\ &= \int_{-2^N T_s}^{0} \frac{V_{IN,-} + V_{IN,\sim}}{RC} d\tau \\ &= \frac{V_{IN,-}}{RC} \cdot 2^N T_s + \int_{-2^N T_s}^{0} \frac{V_{IN,\sim}}{RC} d\tau. \end{aligned} \tag{2.12}$$

The last term in Eq. 2.12 is zero only if the frequency dependent component $V_{IN,\sim}$ has an integer number of cycles in $2^N T_s$ seconds. Otherwise, some part of $V_{IN,\sim}$ will alter the desired voltage at V_{INT}. This can be seen by assuming one of the frequency dependent components of $V_{IN\sim}$ is of the form $A\cos(\omega t)$. The integral of the last term will be

$$\int_{-2^N T_s}^{0} \frac{A\cos(\omega t)}{RC} d\tau = \frac{A\sin(\omega 2^N T_s)}{\omega} = \frac{A \cdot 2^N T_s \sin(\omega 2^N T_s)}{\omega 2^N T_s}. \tag{2.13}$$

This function is plotted in Fig. 2.7 where the period is $T = 2^N T_s$. When ω is equal to integer multiples of $1/T = 1/2^N T_s$, the frequency dependent signal $V_{IN\sim}$ is suppressed by the nulls in the spectrum. For non-integer multiples of $1/2^N T_s$, the signal $V_{IN\sim}$ will not be suppressed and will affect the final output of the dual-slope A/D converter.

2.2.2 First-Order Incremental A/D Converters

The architecture of an incremental A/D converter is almost identical to that of a $\Delta\Sigma$ modulator except the integrators are reset after each conversion, the input is held for each conver-

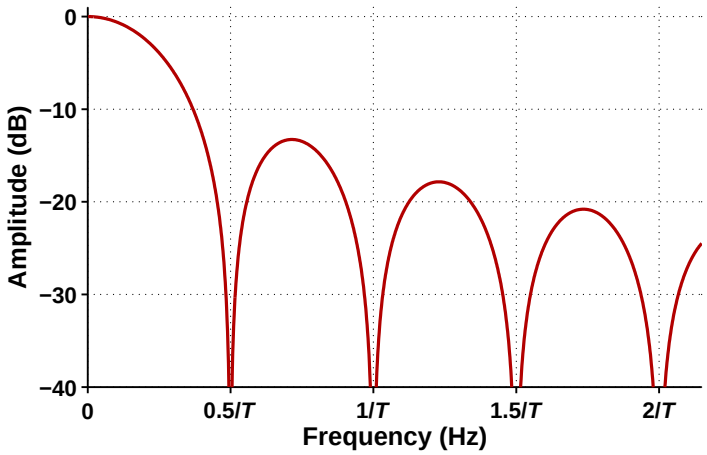


Figure 2.7: Function $AT\sin(\omega T)/\omega T$ (the peak amplitude AT is normalized to 0 dB). The spectral nulls are evident at integer multiples of π for the argument ωT. For the dual-slope A/D converter, $T = 2^N T_s$.

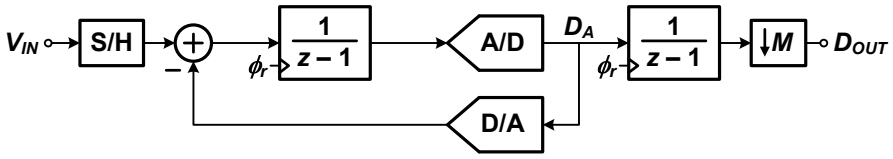
sion[1], and the decimation filter is different. However, a 1st-order incremental A/D converter is better understood as operating like a dual-slope A/D converter since the input/output relationship is identical. Also, like a dual-slope A/D converter (and similar to a Nyquist-rate A/D converter), input signals that fall between $f_s/(2 \cdot OSR)$ and $f_s/2$ alias back into the signal band and are not suppressed by the digital decimation filter as they would be in a $\Delta\Sigma$ modulator.

A 1st-order incremental A/D converter is shown in Fig. 2.8. In contrast to a dual-slope A/D converter, the integration and subtraction of the reference signal are mixed in time. This is apparent if the 1-bit D/A converter output is either V_{REF} or 0 and the A/D threshold is V_{REF}. Assuming a positive unipolar input, the constant input is integrated until it is larger than V_{REF}. At this point, V_{REF} is subtracted from the input, and the counter is incremented by 1. This continues for 2^N-1 clock cycles to obtain a resolution of N bits (this is half as many as a dual-slope converter because a 2-phase clock is used). Once the conversion is performed (after OSR clock cycles), the integrator is reset and the next sample is converted. An added benefit to incremental A/D converters is the simplicity of the decimation filter.

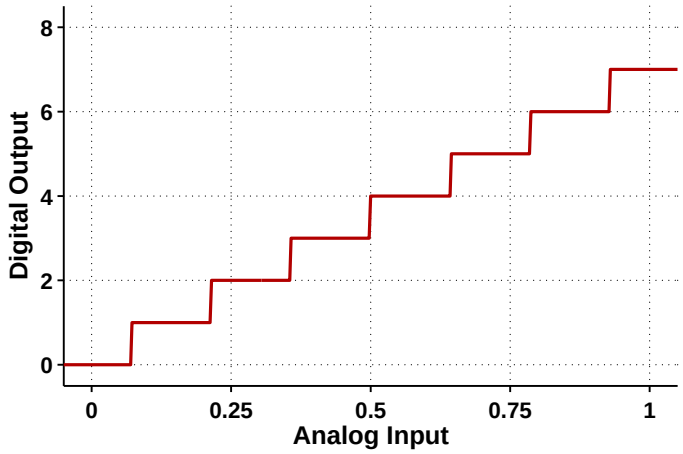
[1] It is assumed that the input is held to attain the ideal behaviour of an incremental A/D converter. However, for instrumentation applications this is not always done in practice. Much like the dual-slope A/D converter it is advantageous to introduce spectral nulls at specific frequencies, which is accomplished by using a moving input and adjusting the sinc decimation filter [46]. This requires a more complicated decimation filter.

It can be as simple as a cascade of L accumulators for an L^{th}-order converter (as shown in Fig. 2.8), although more complicated filters can be used [46–48].

An example of the converter output is shown in Fig. 2.8 for 7 cycles, resulting in a 3-bit or 8-level output. While the incremental A/D converter is an oversampled A/D converter, its characteristics are more similar to that of a Nyquist-rate A/D converter because input signals larger than $f_s/(2 \cdot OSR)$ will alias back into the signal band unattenuated, assuming the use of an input *sample-and-hold* (S/H).



(a) Architecture



(b) Output vs. Input Plot

Figure 2.8: Operation of a 1st-order incremental A/D converter with an OSR of 7 and a binary quantizer, resulting in 8 output levels.

An extra bit can be obtained with one extra cycle [49]. Using a first-order incremental A/D converter as an example, the input to the quantizer after M cycles with an N-level quantizer is (see Appendix A, Eq. A.1)

$$V_Q[M] = \sum_{i=1}^{M} V_{IN}[i] - \sum_{i=1}^{M-1} V_{REF} \cdot D_A[i]. \tag{2.14}$$

With one extra cycle while the input is grounded, the resulting input to the quantizer is

$$V_Q[M] = \sum_{i=1}^{M} V_{IN}[i] - \sum_{i=1}^{M} V_{REF} \cdot D_A[i]. \tag{2.15}$$

This is the error between the input signal V_{IN} and the digital output code. This error signal is uniformly distributed and the signal polarity can be evaluated for one extra bit (alternatively, it can be quantized at the same resolution N for $\log_2(N-1)$ additional bits). However, for an OSR as low as 3 an extra clock cycle reduces the bandwidth by 33%. While this becomes less significant at higher OSRs, with an OSR of 3 this is not a worthwhile trade-off since the target application is high speed, and resolution can be achieved using other means (for example, using higher resolution quantizers or higher order converters).

In some cases the incremental A/D converter is considered a $\Delta\Sigma$ modulator operating in transient mode [50]. At high oversampling ratios, the longer an incremental A/D converter operates after the reset phase, the more similar its internal states becomes to that of a $\Delta\Sigma$ modulator, and after an infinite number of clock cycles its internal operation is identical to that of a $\Delta\Sigma$ modulator. However, at low OSRs (for example, an OSR of 3), it is most appropriate to think of an incremental A/D converter as operating distinctly from a $\Delta\Sigma$ modulator. While the loop filter may look similar, in many ways it operates more like a Nyquist-rate A/D converter; noise-shaping no longer occurs (see Section 2.2.4 for noise analysis), and signals out of band get aliased back into the signal band.

While the decimation filter of an incremental A/D converter can be as simple as a cascade of L accumulators for an L^{th}-order converter, there are more optimal ways to filter the digital data. [46] suggests the use of a dither signal in the analog loop filter along with a higher-order cascade of accumulators ($L+1$) to improve the resolution. [47] presents an optimal decimation filter that both minimizes the maximum error and the mean-squared error. These filters come at the cost of increased digital complexity.

2.2.3 Higher-Order Incremental A/D Converters

$\Delta\Sigma$ modulator techniques can be applied to incremental A/D converters. If the OSR of an incremental A/D converter is defined as the number of cycles in one conversion, then it is clear that an increased OSR will increase the resolution. Unlike dual-slope A/D converters, incremental A/D converters can utilize higher-order loop filters to further increase

the resolution. Higher-order incremental A/D converters can be implemented in either a single-stage structure, or a cascaded architecture.

Single-Stage Incremental A/D Converters

Single-stage architectures suffer from increased signal swings at the integrator outputs [49], but low-distortion input feed-forward architectures [39, 46] can be used to reduce these signal swings. Fig. 2.9 illustrates a 2nd-order single-stage incremental A/D converter with an NTF of $(1-z^{-1})^2$ and a bipolar input. The resulting output vs. input characteristics are also shown for an OSR of 7, as well as the *differential non-linearity* (DNL) error. The single-stage architecture has 29 output levels, but these levels are only suitable for inputs within +/- 0.6. Beyond that, the DNL error is greater than 0.5 LSB. The DNL error occurs due to the restriction on the input signal amplitude for higher-order incremental A/D converters in the same way that ΔΣ modulators are only stable for a given input signal amplitude.

At high OSRs, the valid input range for incremental A/D converters is similar to ΔΣ modulators which are governed by [4]

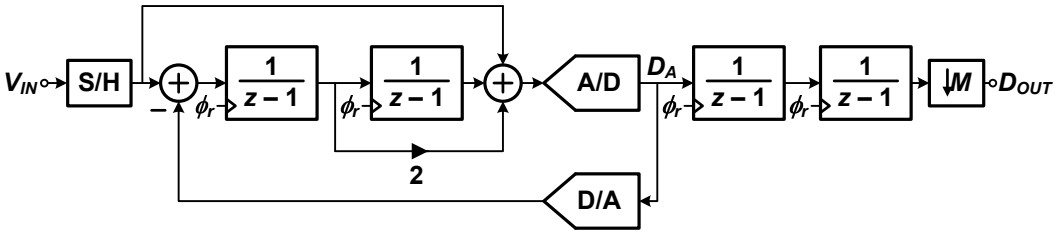
$$\max|V_{IN}| = \frac{N+1-\|h(n)\|_1}{N-1} \tag{2.16}$$

for an N-level quantizer where $\|h(n)\|_1$ is the first norm[2] of the NTF $H(z)$. For the 2nd-order modulator shown in Fig. 2.9, $\|h(n)\|_1 = 4$, and it is clear that the input to a single-bit quantizer where $N = 2$ is never guaranteed to be stable unless the NTF is modified. When the input is in the stable input range (assuming an NTF of the form $(1-z^{-1})^L$), the output will be identical to the ideal staircase output and the DNL will be zero. However, depending on the OSR, simulation can verify that the output may still have an acceptably low DNL in a larger range, as is the case for the single-stage architecture in Fig. 2.9.

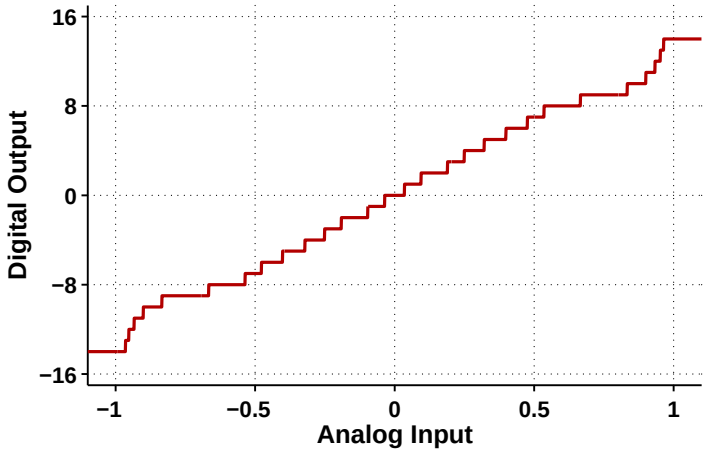
For a single-stage architecture with an NTF of the form $(1-z^{-1})^L$, the resolution can be found using the following equation for the number of output levels [51] (see Appendix A)

$$N_{\text{inc,ss}} = \alpha(N-1)\frac{(M+L-1)!}{L!(M-1)!}+1 \tag{2.17}$$

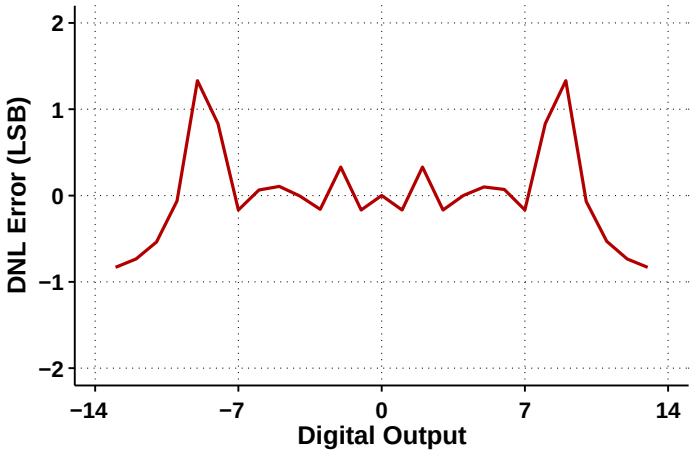
[2]For a filter $H(z) = h_0 + h_1 z^{-1} + \ldots + h_{N-1}z^{-N+1}$, the first norm (or L^1 norm) is $\sum_{i=0}^{N-1}|h_i|$.



(a) Architecture



(b) Output vs. Input Plot



(c) DNL Error Plot

Figure 2.9: Operation of a 2nd-order single-stage incremental A/D converter with an OSR of 7 and a binary quantizer, resulting in 29 output levels.

for an L^{th}-order converter with N quantizer levels and an OSR of M, where the resolution is $\log_2(N_{\text{inc,ss}})$ bits. The coefficient α is the maximum converter amplitude that keeps the quantizer input bounded and is usually less than unity.

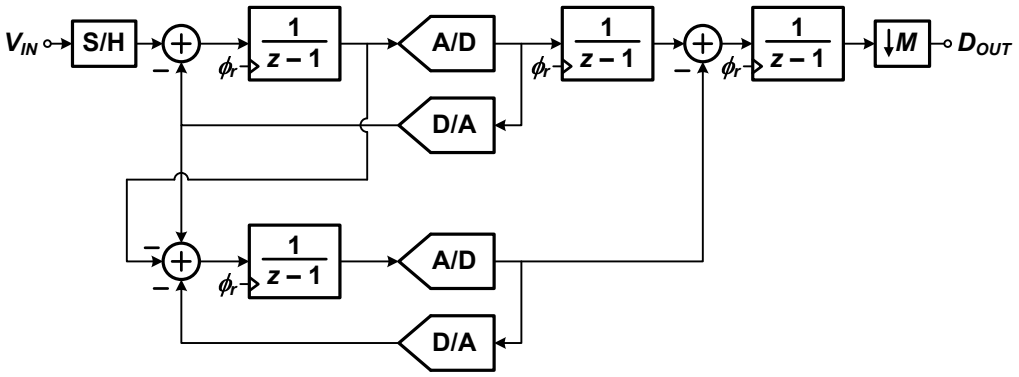
Cascaded Incremental A/D Converters

Like $\Delta\Sigma$ modulators, the cascaded architecture is more stable for higher-order converters. As opposed to feeding the first integrator output into the subsequent stage (as suggested in [49]), the first stage error can be fed into the following stage. This results in a smaller signal amplitude being fed to the subsequent stage since it has less signal component [39], and facilitates the use of interstage gains and multi-bit quantizers to increase the SQNR.

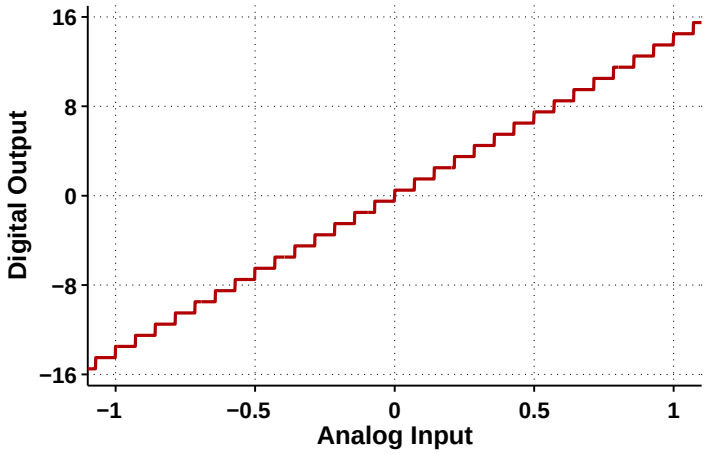
Fig. 2.10 illustrates a 2^{nd}-order cascaded incremental A/D converter with an NTF of $(1-z^{-1})^2$. For the same NTF as in Fig. 2.9, the cascaded architecture has 30 output levels for an OSR of 7, and they form a perfect staircase output. Since the maximum stable input amplitude is unity, no DNL error occurs for the entire input range. The single-stage incremental converter of Fig. 2.9 would need another comparator to have a similar number of output levels as the cascaded incremental converter. However, while the total number of comparators in each architecture would be the same, the single-stage architecture would not have the same stable input range (as expected from Eq. 2.16). Also, the single-stage incremental converter would required larger comparators to accommodate higher resolution within its single quantizer (this is not the case with the cascaded architecture since the quantizer resolution is spread across two lower resolution quantizers).

It can also be seen that the input extends beyond unity and the perfect staircase is still intact. Instability results due to quantizer overload, but the quantizer in an incremental converter may not overload at lower OSRs since it is reset every OSR clock cycles, meaning that the accumulation responsible for quantizer overload is cut short, unlike in $\Delta\Sigma$ modulators. This allows slightly larger full-scale inputs than would be expected in an equivalent NTF for a $\Delta\Sigma$ modulator.

The cascaded architecture that will be discussed in this paper is an L^{th}-order cascade of 1^{st}-order stages with NTFs of $(1-z^{-1})^L$. The resolution (in bits) of this particular cascaded architecture is $\log_2(N_{\text{inc,casc}})$ and can be computed from the number of output levels (see



(a) Architecture



(b) Output vs. Input Plot

Figure 2.10: Operation of a 2nd-order cascaded incremental A/D converter with an OSR of 7 and 30 output levels.

Appendix A)

$$N_{\text{inc,casc}} = \alpha(N-1)^L \frac{(M+L-1)!}{L!(M-1)!} + 1 \tag{2.18}$$

where M is the OSR, N is the number of quantizer levels and α is the product of the maximum converter input that keeps the quantizer bounded for each stage. Since the 1st-order incremental A/D converter does not overload with inputs as large as unity, α will be unity or slightly larger. Eq. 2.18 assumes that an interstage gain of $N-1$ is used between cascaded stages.

2.2.4 Input-Referred Noise

Calculating the input-referred noise in an incremental A/D converter is quite different from a ΔΣ modulator. Every conversion has a weighting associated with each sample, and for higher-order modulators earlier samples have a higher weighting than later samples [46,52]. The total input-referred noise power $\overline{v_n^2}$ is

$$\overline{v_n^2} = \sum_{i=1}^{M} w_i^2 \overline{v_s^2} = \overline{v_s^2} \sum_{i=1}^{M} w_i^2 \tag{2.19}$$

where $\overline{v_s^2}$ is the input noise power of each sample, M is the OSR (and number of samples per conversion), and w_i is the weighting associated with each sample.

In a 1st-order modulator, the weighting factors are equal ($w_i = 1/M$) since the output is effectively an average of the M inputs added to the quantization noise error introduced. The resulting input-referred noise power is $\overline{v_n^2}/M$, as expected for an A/D converter oversampled by M. However, as the modulator order increases, this is no longer the case. For a 2nd-order modulator, the weighting factors increase to

$$w_i = \left\{ \frac{1}{M(M+1)/2}, \frac{2}{M(M+1)/2}, \ldots, \frac{M}{M(M+1)/2} \right\}. \tag{2.20}$$

The resulting total noise power is increased by a factor of up to 4/3 [46] since

$$\sum_{i=1}^{M} w_i < \frac{4/3}{M}. \tag{2.21}$$

At an OSR of 1, this reduces to the expected $1/M$, but for higher OSRs these higher-order incremental A/D converters introduce more input-referred noise into the system when compared to ΔΣ modulators, to a maximum of 33%.

The additional noise can be compared for modulators of various orders and OSRs, and the results are summarized in Table 2.1. It is clear that at high OSRs, lower-order incremental A/D converters must be used to keep the input-referred noise power low. However, when low OSRs are used, there is a limit on the converter order to maintain a given noise power. Note that the preceding weighting factors assume a digital decimation filter of the form $(1-z^{-1})^L$.

Order	Oversampling Ratio							
	1	2	4	8	16	32	64	128
1	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
2	1.00	1.11	1.20	1.26	1.29	1.31	1.32	1.33
4	1.00	1.36	1.69	1.93	2.09	2.18	2.23	2.26
8	1.00	1.60	2.32	2.99	3.51	3.85	4.05	4.15
12	1.00	1.72	2.68	3.74	4.67	5.35	5.77	6.00

Table 2.1: Relative input-referred noise power for incremental A/D converters for various OSRs and orders. The results are normalized to the expected input-referred noise power for an oversampled A/D converter where the noise is $1/M$ for an OSR of M.

2.3 Pipeline Data Converters

The design of pipeline data converters can be similar to switched-capacitor realizations of $\Delta\Sigma$ modulators or incremental A/D converters. For a given technology the maximum sampling frequency of a discrete-time pipeline A/D converter and $\Delta\Sigma$ modulator are similar, as shown in Table 1.1 and Table 1.2. As the OSRs of $\Delta\Sigma$ modulators and incremental A/D converters are lowered, it will be seen that the design challenges become similar to those of pipeline A/D converters. For this reason it is important to understand the basic operation and design of pipeline A/D converters.

2.3.1 Architecture

A pipeline A/D converter cascades several individual low-resolution stages in such a way that the overall resolution (in bits) is roughly the sum of each individual stage's resolution (in bits). Redundancy is employed to reduce the offset requirements of the A/D comparators within each individual stage that could otherwise limit the performance of the entire converter.

A single stage of a pipeline A/D converter is shown in Fig. 2.11. The input is quantized in a low resolution flash A/D converter, converted back to an analog signal, and then subtracted from the analog input V_{IN} leaving only the error E_1 introduced by the flash A/D converter to be passed on to the subsequent stage. An interstage gain factor G can be used

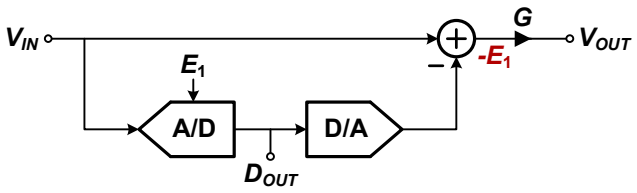


Figure 2.11: Individual stage of a pipeline A/D converter.

if the error signal does not utilize the full input range of the subsequent stage.

Multiple stages are cascaded in such a way that the previous stage error signal acts as the input to the current stage. The digital outputs of every stage are collected and manipulated digitally to create a final digital output, based on the interstage gain factor G. This is shown in Fig. 2.12 where the final digital output is

$$D_{OUT} = D_1 \prod_{i=1}^{n} G_i + D_2 \prod_{i=2}^{n} G_i + \ldots + D_n \prod_{i=n}^{n} G_i. \tag{2.22}$$

Also shown in Fig. 2.12 is a S/H on the input. This is necessary to ensure that the signal sampled by the internal A/D of the first stage is the same as the input sampled at the summer. The converter input V_{IN} is a continuous-time signal and a mismatch in the delay of both paths will cause an error in the signal passed to the next stage. With a S/H at the input, the internal signals are discrete-time and slight mismatches in the sampling clock do not cause an error. For stages beyond the first, the internal signals are already discrete-time so this is not an issue. This will be discussed further in Section 5.3.3.

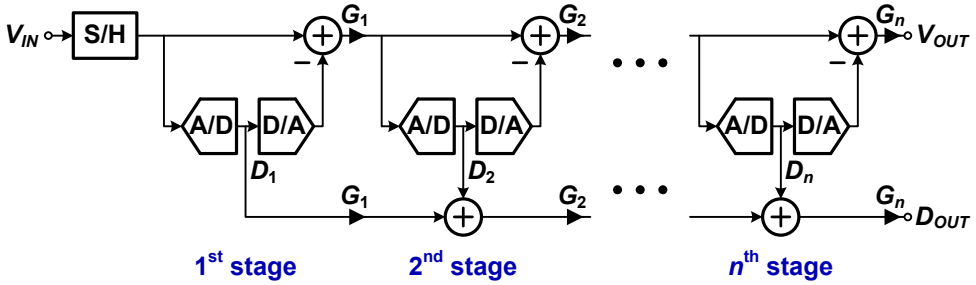


Figure 2.12: Architecture of a pipeline A/D converter.

The resolution of a single-stage in a pipeline A/D converter is equal to the N-level

internal A/D resolution. For multiple stages, the total number of output levels is

$$N_{total} = \prod_{i=1}^{n}(N_i - 1) + 1. \tag{2.23}$$

Note that this is identical to the number of output levels predicted by Eq. 2.18 when the cascaded incremental A/D converter is operated at an OSR of 1.

2.3.2 Offsets

The internal A/D converters of a pipeline have more levels than necessary. This introduces redundancy which reduces the impact of offsets that would otherwise limit the entire pipeline converter performance. The benefit of redundancy can be seen with an example of a single stage within the pipeline A/D converter architecture. If the n^{th} stage is designed with a resolution of 2 bits, the corresponding error signal $4E_n$ is shown in Fig. 2.13. A gain of 4 utilizes the full-scale range of the subsequent stage. In the presence of comparator offsets, the error signal will go above and below the full-scale range of ± 1, causing distortion in the error signal entering the next stage while also creating an uncorrectable error in the final output code.

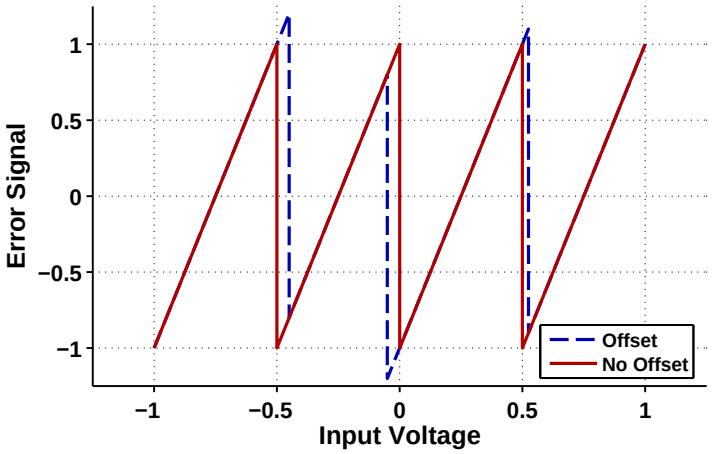


Figure 2.13: Pipeline stage error signal in the presence of comparator offset with 4 comparator levels resolved.

Alternatively, if only 1.5 bits are resolved (i.e., a 3-level A/D), a gain of 2 can be used as shown in Fig. 2.14 [53]. While the full scale is not utilized across the entire comparator

input range, offsets within the comparator only adjust the signal slightly above or below ± 0.5. This is within the input range of the subsequent stage and will not cause distortion in the output. As long as the offset does not cause the output to saturate, then it can be corrected with the subsequent stages, allowing for large offsets within the comparator. The cost of this feature is redundancy within the pipeline, requiring more comparators throughout the converter. The pipeline will not resolve as many bits per stage, resulting in more stages for a given resolution.

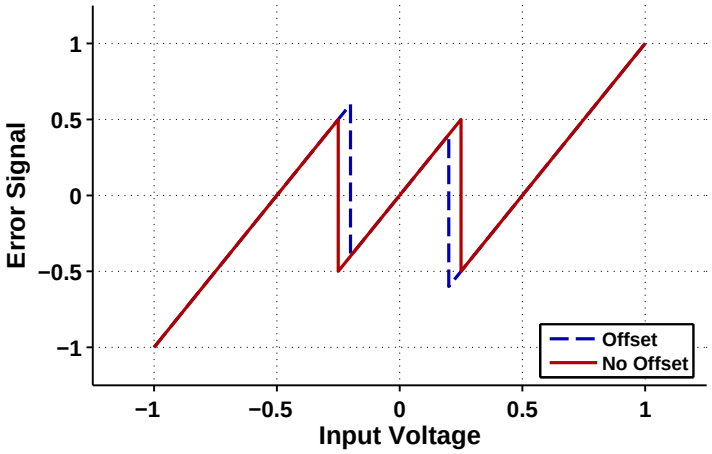


Figure 2.14: Pipeline stage in the presence of comparator offsets with 3 comparator levels resolved.

2.3.3 Cascaded like a MASH

The pipeline A/D converter is similar to a cascaded $\Delta\Sigma$ modulator in that they both require error cancelation. While both architectures generate error signals differently, they both pass error signals from stage to stage, and they both require the digital reconstruction filter to match the gains or integrators of the analog circuits.

When a pipeline A/D converter is redrawn as shown in Fig. 2.15, it is similar to Fig. 2.5. This similarity can help explain how a pipeline A/D converter and a resettable cascaded $\Delta\Sigma$ modulator (i.e., an incremental converter) become almost identical when operated at an OSR of 1. This will be discussed further in Section 4.1.2.

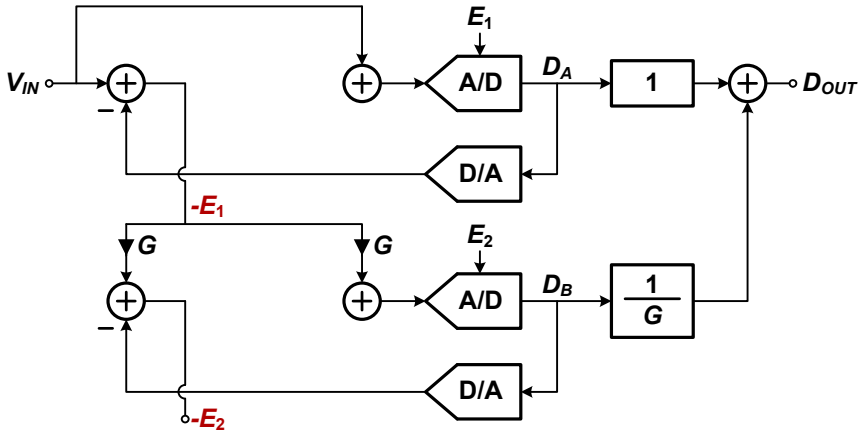


Figure 2.15: Two-stage pipeline redrawn to demonstrate its similarities with a cascaded ΔΣ modulator. The integrators of the cascaded ΔΣ of Fig. 2.5 have been removed to generate this figure.

2.4 Time-Interleaving

2.4.1 Nyquist-Rate A/D Converters

One method for increasing the bandwidth of A/D converters is time-interleaving. Theoretically any number of parallel A/D converters can be put in parallel to increase the throughput of a data converter. The bandwidth increases by the number of parallel A/D converters, at the expense of increased power. In systems where the maximum sampling frequency is limited by the technology, this may be the only way to further increase the bandwidth.

Fig. 2.16 shows the general structure of a time-interleaved Nyquist-rate A/D converter. The input and output multiplexers must operate at the higher bandwidth nf_s while all the internal circuitry operates at f_s. The main difficulties that exist with time-interleaving are matching between the parallel A/D converters, and timing skew between the sampling clocks of these parallel converters [54, 55].

2.4.2 ΔΣ Modulators

Time-interleaving in ΔΣ modulators is more complicated than in regular Nyquist-rate A/D converters. The modulators can be parallelized using block digital filters where cross-coupled paths are used between the parallel paths, but the effective sampling frequency is increased. The effective OSR is increased using this technique, so a lower sampling

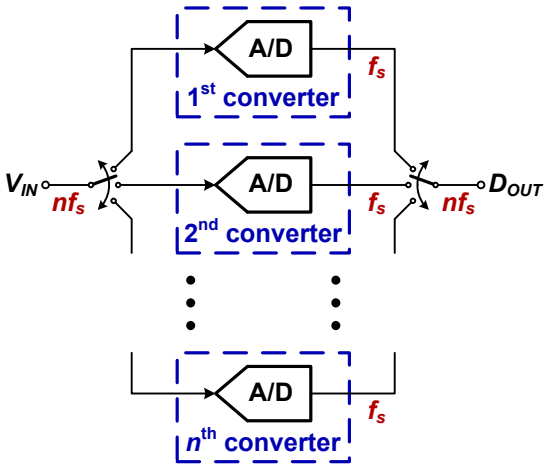


Figure 2.16: Time-interleaved Nyquist-rate A/D converter.

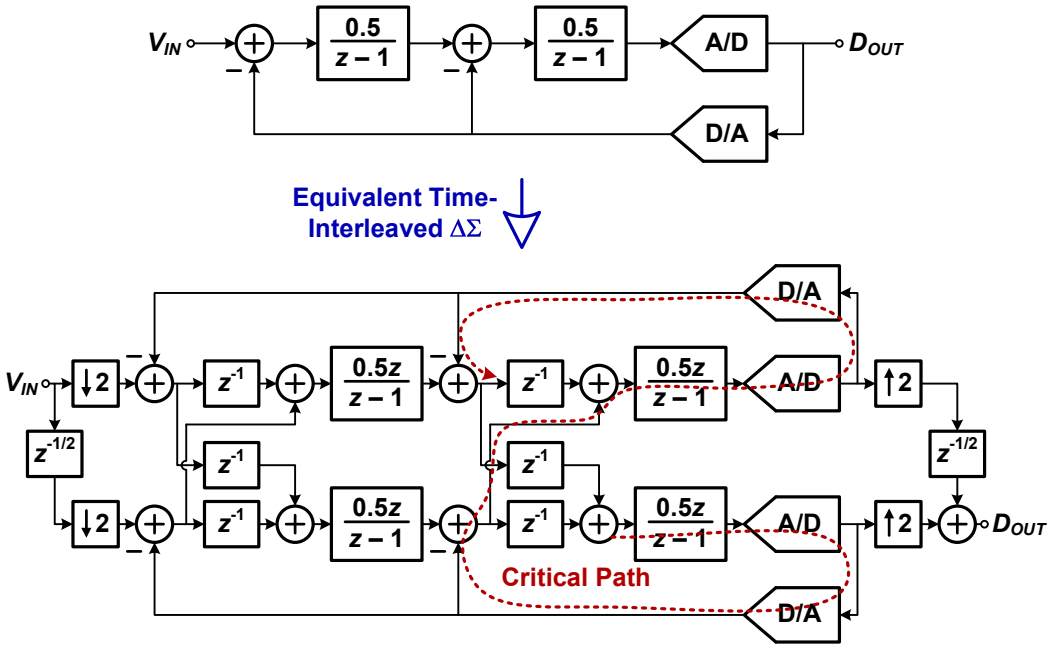


Figure 2.17: Time-interleaved ΔΣ modulator.

frequency for a given SQNR is needed [56]. An example of a 2nd-order time-interleaved by 2 ΔΣ modulator using block digital filtering is shown in Fig. 2.17.

The major difficulty with this technique when trying to time-interleave more than two

modulators is the critical path highlighted in Fig. 2.17. This path has no delays and works when time-interleaved by 2 because there is a two-phase clock inherent in discrete-time switched-capacitor implementations. Alternatively, continuous-time architectures can be used where the feedback pulse timing is shaped to overcome the critical path [12]. When more than two parallel modulators are combined, other techniques must be used to overcome the critical path [57,58] which may introduce images of the input signal in the output spectrum [59].

2.5 A/D Trade-Offs: Power, Resolution and Bandwidth

The fundamental trade-offs in data converters are important to properly design power efficient converters. Power, bandwidth, and resolution are the three main trade-offs and their relationship to each other will be briefly discussed. It is assumed that resolution is limited by thermal noise, which is typical of medium to high resolution A/D converters operating in the megahertz range.

Throughout the chapters, power will often be traded with bandwidth or resolution to compare similar architectures with different OSRs. These relationships are discussed in the following sections.

2.5.1 Power and Bandwidth

Power and bandwidth are proportional to each other. An increase in bandwidth will cause a proportional increase in power with the resolution kept constant. Time-interleaving is a simple example of this relationship; with two identical converters time-interleaved, the resulting bandwidth and power are both doubled. The resolution remains the same as the resolution of the individual converters. Fig. 2.18 illustrates this trade-off.

The trade-off ignores the power required to combine the digital outputs, or the power required to calibrate or design the converters with greater matching performance. It can be assumed that these effects are small, especially when the power consumption and size of the individual converters are increased relative to the digital logic power.

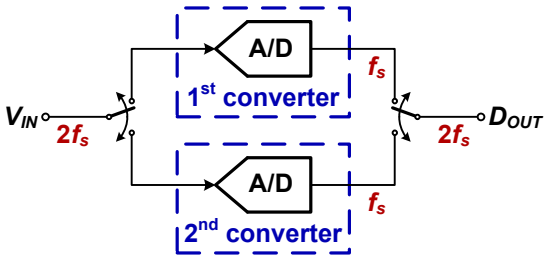


Figure 2.18: Time-interleaved example of the power and bandwidth trade-off. Two time-interleaved converters double the power, but also double the throughput.

2.5.2 Bandwidth and Resolution

Decreasing the bandwidth by a factor of X increases the resolution by a factor of $10\log_{10} X$ if the power is kept constant. An example of this relationship is oversampling. For a thermal noise limited A/D converter output, oversampling by 2 decreases the bandwidth by a factor of 2. This also decreases the total in-band noise by 3 dB, a factor of 2 in power, since only half the spectrum is needed.

Oversampling by 2 effectively filters out half the noise in the output spectrum. This is shown in Fig. 2.19. Again it is assumed that the digital logic power required to create a brick-wall low-pass filter is ignored, but this can be arbitrarily small relative to a large A/D converter and is not a fundamental limitation.

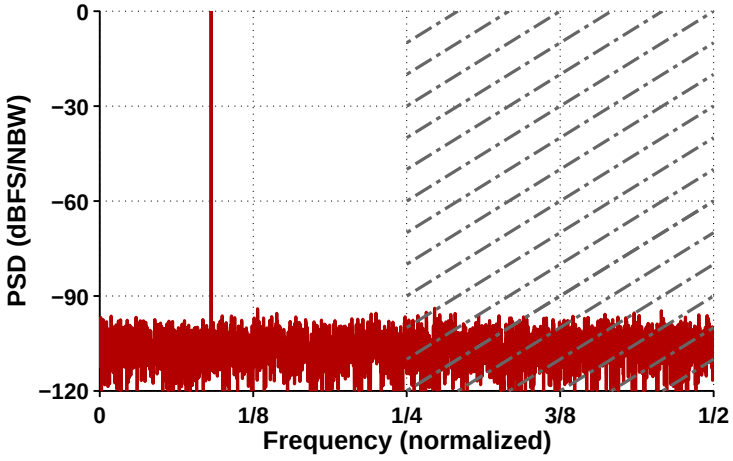


Figure 2.19: Oversampling example of the bandwidth and resolution trade-off. The second half of the spectrum is perfectly filtered, resulting in half the signal bandwidth, and 3 dB less noise (since half the noise bins are ignored).

2.5.3 Resolution and Power

Given the previous trade-offs, it is no surprise that for an increase in power by X the resolution is increased by $10\log_{10}X$, for a constant bandwidth. This can be seen if two thermal noise limited parallel A/D converters operate on the same samples, as seen in Fig. 2.20 (i.e., not time-interleaved). The digital summation and divide by two are assumed to take minimal power.

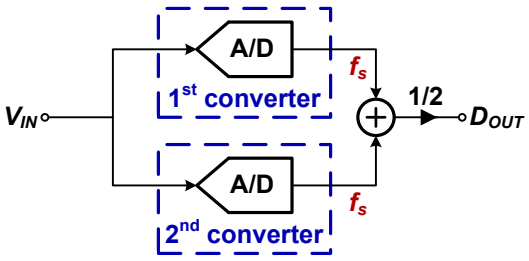


Figure 2.20: Example of the resolution and power trade-off for parallel A/D converters. Two parallel converters double the power, but reduce the noise by 3 dB.

The power is doubled since two A/D converters are used. The signal has the same power since the two branches are added together then divided by two. Since both systems are thermal noise limited, the thermal noise adds as an uncorrelated source, and is then divided by two, resulting in a 3 dB decrease. This results in a corresponding 3 dB resolution increase.

2.5.4 Figure of Merit

The trade-offs presented are supported by the figure of merit shown in [60, 61]

$$\frac{4kT \cdot DR \cdot BW}{P} \tag{2.24}$$

where k is the Boltzmann constant, T is the temperature, DR is the dynamic range (as a power ratio rather than in decibels), BW is the signal bandwidth, and P is the power. The additional temperature dependent term can be ignored when it is assumed that comparisons between different circuits are operating at approximately the same temperature.

Chapter 3

ΔΣ Modulators at Low OSRs

This chapter discusses the operation of ΔΣ modulators at low OSRs. Section 3.1 explains their basic operation at low OSRs, specifically an OSR of 3, and compares them with Nyquist-rate A/D converters. Section 3.2 explores the advantages of cascaded as opposed to single-stage modulators, and Section 3.3 proposes the modulator architecture while discussing it's power efficiency advantages over pipeline A/D converters. Throughout this chapter, an OSR of 3 with 10-bit resolution will be used as the target OSR and resolution for the design.

3.1 Operation at Low OSRs

3.1.1 Increased Noise

It is increasingly difficult to achieve high resolution in ΔΣ modulators at low OSRs. ΔΣ modulation is reliant on oversampled noise-shaping to increase the modulator's resolution, but noise-shaping increases the total quantization noise power in the modulator, and the lower the OSR, the more significant this increased noise power becomes.

As an example, a 2^{nd}-order NTF was shown in Fig. 2.1. The NTF is equal to unity at a normalized frequency of $1/6$. With this filter, the noise introduced above $1/6$ is clearly larger than the noise filtered from the lower frequency between 0 to $1/6$, demonstrating that the total noise throughout the entire frequency band is increased with this NTF.

3.1.2 Comparison with a Nyquist-Rate A/D Converter

Since noise-shaping increases the total noise power in a ΔΣ modulator, at an OSR of 1 a Nyquist-rate A/D converter outperforms a ΔΣ modulator. However, as the OSR increases and less noise power ends up in the band of interest, the SQNR of the ΔΣ modulator improves at a faster rate than the 3 dB per octave improvement from the Nyquist-rate A/D converter. Eventually the ΔΣ modulator will outperform the Nyquist-rate A/D converter.

Fig. 3.1 shows the total in-band integrated noise power (normalized) as a function of the OSR in a 1^{st}-order and 8^{th}-order ΔΣ modulator[1] compared against a Nyquist-rate A/D converter where the normalization assumes the Nyquist-rate A/D converter's quantization noise is the same resolution as the quantization noise introduced into the ΔΣ modulator (before noise-shaping). There is a crossover point depending on the modulator order; for the 1^{st}-order modulator this crossover occurs at an OSR of 1.7, and for an 8^{th}-order modulator it occurs at an OSR of 2.5. This point defines the OSR where it is worth employing noise-shaping rather than simple oversampling for a given modulator order (assuming the same quantizer resolution can be used in both the ΔΣ modulator and the Nyquist-rate A/D converter).

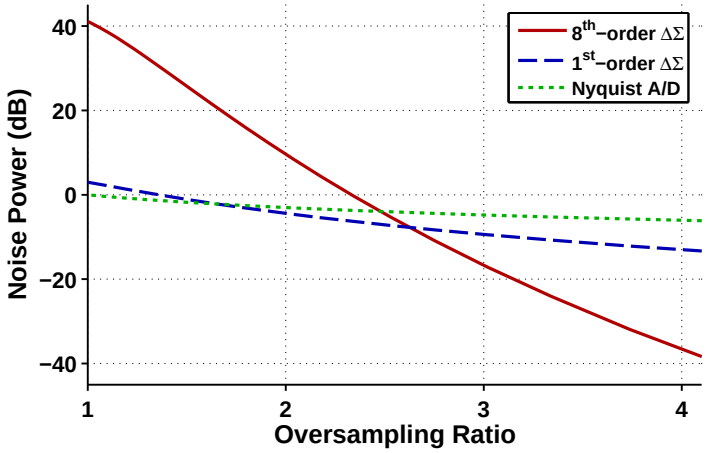


Figure 3.1: Total In-Band Noise Power vs. OSR. The numbers are normalized to a Nyquist-rate A/D converter with an OSR of 1. It is assumed that both A/D converters have the same number of quantizer levels (i.e., same quantization noise power).

[1]The NTFs used in this comparison are $(1-z^{-1})^L$ where L is the modulator order. Also it is assumed that the input can go as large as full-scale, although this would depend on the architecture and quantizer resolution.

The crossover point occurs at lower OSRs for lower-order ΔΣ modulators and the crossover point for various modulator orders is summarized in Table 3.1. Also included in the table is the relative reduction in noise power at an OSR of 3. Despite having a higher crossover OSR for the higher-order modulators, the higher-order modulators still have lower noise powers at an OSR of 3 because the noise power decreases rapidly as the OSR increases. While it may appear that the reduction in noise power is not significant as the modulator order is increased, this table assumes that every architecture has the same quantization noise power. However, higher-order cascaded architectures are more amenable to higher resolution quantizers, resulting in smaller quantization noise power which further reduces the noise power in the modulator. This will be discussed in Section 3.2.

NTF	Crossover OSR	Relative Noise Power (OSR of 3)
1	1	-4.78 dB
$(1-z^{-1})$	1.7	-9.38 dB
$(1-z^{-1})^2$	1.9	-11.53 dB
$(1-z^{-1})^4$	2.2	-14.01 dB
$(1-z^{-1})^8$	2.5	-16.70 dB
$(1-z^{-1})^{12}$	2.6	-18.34 dB

Table 3.1: OSR where noise power in ΔΣ is equal to noise power in Nyquist-rate A/D

3.2 Single-Stage vs. Cascaded ΔΣ

In a ΔΣ modulator, improvements in SQNR come from three main factors: increased OSR, higher resolution in the quantizer, and higher modulator order. For a given OSR, and assuming a maximum quantizer resolution of about 4 to 5 bits (to preserve the simplicity of the design), the modulator order is the most influential degree of freedom for the designer, as well as its associated NTF.

Since the SQNR is reduced with low OSRs, the modulator order must be increased for medium to high resolution ΔΣ modulators. Both single-stage and cascaded ΔΣ modulators

are capable of realizing the same high-order NTFs, but cascaded ΔΣ modulators are more stable than single-stage architectures.

3.2.1 Single-Stage Architecture

Increasing the modulator order in single-stage architectures typically requires increased resolution in the quantizer to maintain stability. This can result in unreasonably large quantizers for high-order modulators, making single-stage architectures difficult for low OSR design.

Fig. 3.2 shows the peak SQNR for a 4^{th}-order, 8^{th}-order, and 12^{th}-order single-stage modulator with an OSR of 3 and quantizer resolutions that vary from 3- to 1025-levels (approximately 10 bits) using the ΔΣ Toolbox [62]. For higher-order modulators (8^{th}- and 12^{th}-order), a minimum quantizer resolution of 5-bits is necessary for an SQNR of at least 62 dB, or 10 bits. The 4^{th}-order modulator (and lower order modulators) would need quantizer resolutions of 65-levels or larger for a 10-bit modulator, which is prohibitively large since a flash A/D converter with such high resolution would take more power and require large comparators for well-matched devices, increasing the power consumption of the latter stages in the ΔΣ modulator.

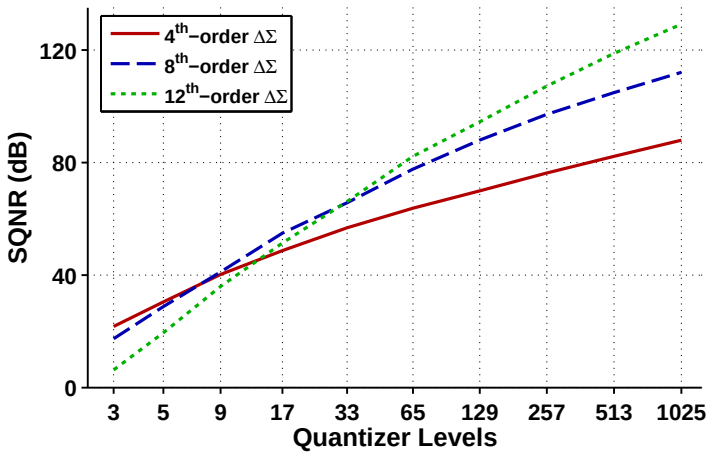


Figure 3.2: SQNR vs. Quantizer Levels. The maximum achievable SQNR for a 4^{th}-order, 8^{th}-order and 12^{th}-order ΔΣ modulator at an OSR of 3.

3.2.2 Cascaded Architecture

A cascaded architecture can realize the same NTFs as single-stage architectures, but they are more stable since each individual stage can be of lower order, and stability of the entire modulator is a function of the individual stages' stability. This results in a larger full-scale input signal, as well as smaller quantizer resolutions in the individual stages which can still cascade to a total resolution larger than that of a single-stage architecture.

However, the difficulty with cascaded architectures is their reliance on matching between the analog and digital circuitry. The digital circuitry in a cascaded ΔΣ must match the analog filters (integrators) for the appropriate noise cancelation to occur. This is increasingly difficult at lower OSRs since input-referred errors are more significant, but it is a familiar problem to Nyquist-rate pipeline A/D designers where the digital gains must match the analog gain circuits. The problem and solution are no different for a high-order cascaded ΔΣ modulator; either the OTA gain and capacitor matching must be sufficient, or calibration is required.

3.3 Proposed High-Order Cascaded ΔΣ

3.3.1 Architecture

If a large number of 1^{st}-order 3-level quantizer ΔΣ stages are cascaded, each individual stage is stable with a full-scale input. The quantizer resolution does not need to be increased to improve stability, and an interstage gain factor of 2 can be used between each stage to increase the resolution of the entire modulator. Each interstage gain of 2 increases the SQNR by 1 bit.

The chosen architecture for this work is an 8^{th}-order cascaded ΔΣ modulator with an OSR of 3 that cascades eight 1^{st}-order ΔΣ stages with 3-level quantizers resulting in an NTF of $(1-z^{-1})^8$. The architecture is shown in Fig. 3.3. Every stage is designed identically, making it relatively simple to implement for an 8^{th}-order modulator. Each individual stage has an input feed-forward path to reduce the input-dependent signal at the integrator output. There is an interstage gain of 2 between each stage, increasing the SQNR by 7 bits (when compared to the same architecture without interstage gains).

An 8^{th}-order single-loop architecture could also obtain the same NTF of $(1-z^{-1})^8$,

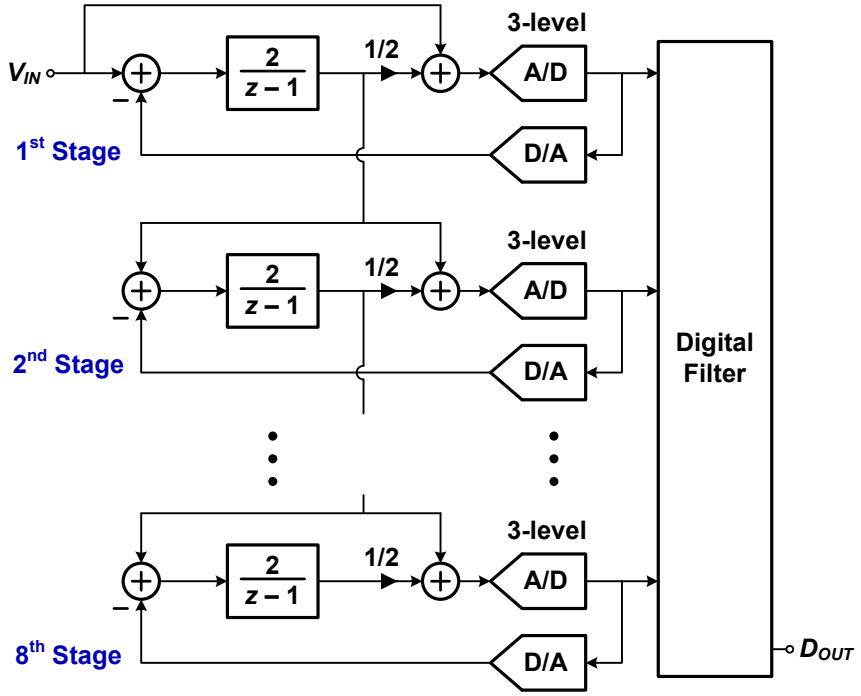


Figure 3.3: 8th-order cascaded ΔΣ architecture. Each of the 8 stages is designed identically with a 3-level quantizer and a weighted summer at the quantizer input.

but it has a few disadvantages. With a 257-level quantizer (which is equivalent to an 8-stage cascade of 3-level quantizers with interstage gains of 2) the modulator full-scale is -14 dBFS, as opposed to 0 dBFS for the cascaded architecture. Not only does this reduce the resolution by 14 dB, but it requires the unreasonably large 257-level quantizer. There are better ways to implement an 8th-order single-loop transfer function (for example, optimized zeros, optimal pole placement), but if the NTFs are kept the same it is clear that a cascaded architecture is far more suitable to low OSR design.

A sample output spectrum of the 8th-order cascaded ΔΣ is shown in Fig. 3.4. The architecture achieves a peak SQNR of 66 dB. The NTF is not optimized for the OSR because only 1st-order stages are used; 2nd-order stages would be necessary to create resonator structures that optimize the NTF zeros, but this aspect of the design remains a future topic for investigation.

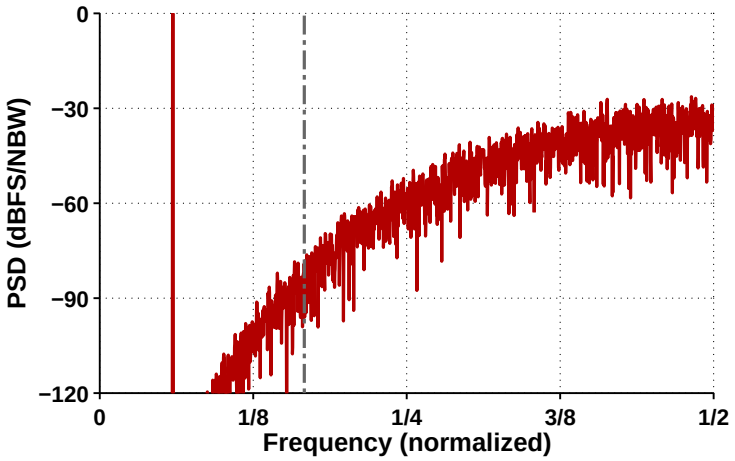


Figure 3.4: Output spectrum for an 8^{th}-order cascaded ΔΣ (NBW $= 3.7 \times 10^{-4}$).

3.3.2 Power Efficiency

It will be shown that the proposed architecture is more power efficient than a comparable Nyquist-rate A/D converter, specifically a 1.5 bit/stage pipeline A/D converter. These two architectures are almost identical in that each requires one OTA per stage and one 3-level quantizer per stage. Also, assuming a power efficient design, they should both be thermal noise limited.

Input-Referred Noise

A large fraction of the power for switched-capacitor thermal noise limited A/D converters is from the first stage, and it should be equally power efficient irrespective of the targeted speed or resolution of the switched-capacitor circuit (assuming similar topologies, to a first-order approximation). The first stage of any A/D converter with a given resolution and bandwidth requires the same amount of analog power, whether it is oversampled or not. Since the sampling capacitor of an oversampled modulator is OSR times less than that of a Nyquist-rate pipeline A/D converter, the power required by the OTA of the oversampled modulator is OSR times less, but since the sampling frequency is OSR times more, the resulting power is equivalent.

When the power of subsequent stages is included, the more power efficient architectures

are those with a lower input-referred noise from later stages. Generally, ΔΣ modulators will have lower input-referred noise from later stages when compared to pipeline A/D converters since the noise from subsequent stages is input-referred through integrators rather than gain stages. Fig. 3.5 shows the input-referred noise through a gain stage and an integrating stage. At an OSR of 3 the two gains are the same, but the total input-referred noise is the area under the curves in the signal band and is less in the integrator/ΔΣ case. However, other input-referred parameters (such as linearity and settling accuracy) are no different at an OSR of 3 because they must be designed for the worst case at the signal band edge, resulting in the same requirements for both a pipeline A/D converter and a ΔΣ modulator.

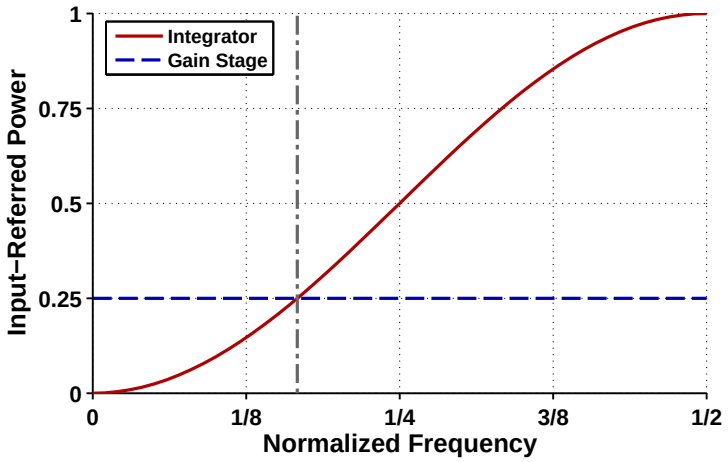


Figure 3.5: Input-referred noise comparison through a gain stage and an integrator stage. At an OSR of 3, the gain is equivalent at the signal band edge, but increasingly less for the integrator stage at higher OSRs.

As an example, if an 8^{th}-order input feed-forward cascaded ΔΣ with an OSR of 3 is compared against a 10-stage, 1.5-bit/stage pipeline A/D converter operating at the same sampling frequency with the same OSR of 3, then both A/D converters will have 66-67 dB of SQNR while the required analog circuitry for these architectures is similar (although the pipeline A/D converter has two extra stages at the end). It is assumed that the pipeline A/D converter can do without the input S/H, a fair assumption given that the input feed-forward cascaded ΔΣ has no S/H and should be similarly reliant on the matching of both input paths. If the design is such that the second and third stages are 2 times smaller than the first stage, and the fifth to last stages are 8 times smaller, then for the same input-referred noise the

pipeline A/D converter consumes 60% more power.

If the first stage is normalized to a size of 1, the total size of the pipeline A/D converter is

$$1+\frac{1}{2}+\frac{1}{2}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}=2.875$$

while the total size of the cascaded ΔΣ modulator is

$$1+\frac{1}{2}+\frac{1}{2}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}+\frac{1}{8}=2.625.$$

With the first stage input-referred noise normalized to 1 (with no oversampling), the total input-referred noise from the 10-stage pipeline is (in the form of $\frac{1}{\text{OSR}}\cdot\text{Noise}\cdot(\text{Input-Referred Gain})^2$)

$$\begin{aligned}&\frac{1}{3}\cdot 1\cdot\frac{1}{1^2}+\frac{1}{3}\cdot 2\cdot\frac{1}{2^2}+\frac{1}{3}\cdot 2\cdot\frac{1}{4^2}+\frac{1}{3}\cdot 8\cdot\frac{1}{8^2}+\frac{1}{3}\cdot 8\cdot\frac{1}{16^2}+\frac{1}{3}\cdot 8\cdot\frac{1}{32^2}\\&+\frac{1}{3}\cdot 8\cdot\frac{1}{64^2}+\frac{1}{3}\cdot 8\cdot\frac{1}{128^2}+\frac{1}{3}\cdot 8\cdot\frac{1}{256^2}+\frac{1}{3}\cdot 8\cdot\frac{1}{512^2}=0.597\end{aligned}$$

while the input-referred noise from the 8-stage cascaded ΔΣ is (in the form of $\frac{1}{\text{OSR}}\cdot\text{Noise}\cdot(\text{Input-Referred Gain})^2\cdot\text{Gain-to-Integrator Factor}$)

$$\begin{aligned}&\frac{1}{3}\cdot 1\cdot\frac{1}{1^2}\cdot\frac{1}{1}+\frac{1}{3}\cdot 2\cdot\frac{1}{2^2}\cdot\frac{1}{2.89}+\frac{1}{3}\cdot 2\cdot\frac{1}{4^2}\cdot\frac{1}{4.74}+\frac{1}{3}\cdot 8\cdot\frac{1}{8^2}\cdot\frac{1}{6.57}+\frac{1}{3}\cdot 8\cdot\frac{1}{16^2}\cdot\frac{1}{8.40}\\&+\frac{1}{3}\cdot 8\cdot\frac{1}{32^2}\cdot\frac{1}{10.22}+\frac{1}{3}\cdot 8\cdot\frac{1}{64^2}\cdot\frac{1}{12.04}+\frac{1}{3}\cdot 8\cdot\frac{1}{128^2}\cdot\frac{1}{13.86}=0.408\end{aligned}$$

where the Gain-to-Integrator Factors were found through numerical integration. The input-referred noise of the pipeline A/D converter is 46% more, and taking into account the extra 10% power for the 2 extra stages, the total additional power of the pipeline A/D converter is 60%.

Clocking Efficiency

The assumption that the first stage power will be the same assumes a similar clocking scheme. However, the cascaded ΔΣ architecture has the flexibility of using full-period delaying integrators with each stage clocked on ϕ_1. On the contrary, pipeline A/D converters are constrained to using half-delaying gain stages since a half clock cycle is needed to reset the previous value on the gain stage (i.e., odd stages of the pipeline sample on ϕ_1, even

stages of the pipeline sample on ϕ_2). Half-delaying gain stages are power inefficient when the subsequent stage has a similarly sized capacitor because the subsequent stage loads the current stage while it is in the amplifying/integrating phase, and this phase typically limits the OTA bandwidth since power efficient designs have a switch resistance that is smaller than $1/G_m$ of the OTA. To charge the subsequent stage's sampling capacitance, extra current must be drawn from the amplifier, resulting in a larger amplifier. Also, a larger amplifier causes a reduced feedback factor β, further increasing the amplifier size for a given settling time constant.

Comparing the same 1.5 bit/stage pipeline A/D converter against the architecturally similar 8^{th}-order cascaded ΔΣ, the power savings from full-delaying gain stages instead of half-delaying gain stages can be seen. As shown in Fig. 3.6, during the amplification/integrating phase the 3-dB frequency is $\omega_{3dB} = \beta G_m / C_{L,eff}$ where $\beta = C_2/(C_1 + C_2 + C_{IN})$ and for the half-delaying pipeline gain stage

$$C_{L,eff} = C_1/2 + \frac{C_2(C_1 + C_{IN})}{C_1 + C_2 + C_{IN}} \tag{3.1}$$

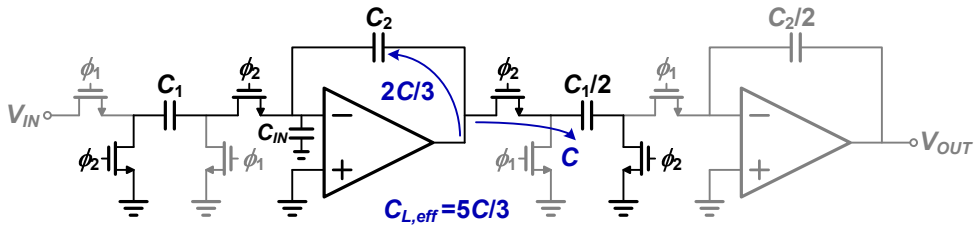
while for the full-delaying ΔΣ integrating stage

$$C_{L,eff} = \frac{C_2(C_1 + C_{IN})}{C_1 + C_2 + C_{IN}}. \tag{3.2}$$

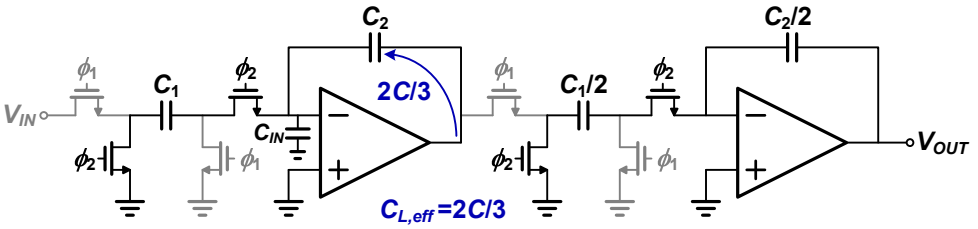
With $C_1 = 2C_2$ (for a 1.5-bit/stage design, or an integrator with a gain of 2), the effective load capacitance $C_{L,eff}$ and OTA power of the delaying stage is 2.5 times less than that of the non-delaying stage for the same ω_{3dB} assuming $C_{IN} = 0$. For increasing values of C_{IN} the disparity becomes larger because the non-delaying stage has a larger OTA than the delaying stage, resulting in larger C_{IN}, smaller β, and decreased OTA efficiency.

It may be considered unrealistic to assume that the ΔΣ stage has no load capacitance on the amplifying phase. However, even if a capacitance equal to 20% of the feedback capacitance C_2 is added as a parasitic capacitance, it still consumes less than half the power of the pipeline OTA for the same ω_{3dB}.

A couple architectural improvements can be used to improve the power efficiency of a pipeline A/D converter. A pipeline A/D gain stage has improved power efficiency with a precision gain stage since it has a reduced feedback factor and load capacitance in the



(a) Non-delaying stages.



(b) Delaying stages.

Figure 3.6: Comparison of non-delaying and delaying stages. The non-delaying stage is typical for pipeline A/D converters while the delaying stage is typical for ΔΣ modulators.

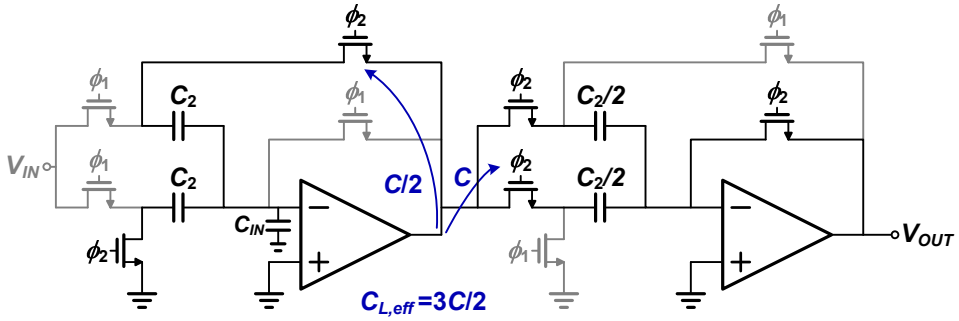


Figure 3.7: Precision delaying gain stage.

amplification phase [63, 64]. This is shown in Fig. 3.7 where $\beta = C_2/(2C_2 + C_{IN})$ and

$$C_{L,eff} = C_2 + \frac{C_2(C_2 + C_{IN})}{2C_2 + C_{IN}}. \tag{3.3}$$

The resulting power is only 50% more with the same ω_{3dB} when compared to the delaying integrators of the ΔΣ modulator.

Other alternatives include powering down the OTA in the sampling phase using the switched-opamp technique [65, 66] or sharing it with a parallel structure [67, 68]. A further

improvement uses the switched-opamp technique while reducing the amplifier loading by using the feedback capacitor of the current stage as the sampling capacitor for the subsequent stage [69]. With these techniques roughly half the power is required for the same ω_{3dB} (except for [69] which has the potential to make further improvements). These techniques are necessary to keep the pipeline A/D converter's power efficiency similar to that which is inherent in the cascaded ΔΣ architecture.

Alternative Gain Distributions

Both the ΔΣ and pipeline architectures will have reduced input-referred noise from later stages if the gain from the first stage to subsequent stages is large. The assumption that the first stage noise will dominate the total noise becomes increasingly valid as the input-referred noise from later stages becomes less significant. In ΔΣ modulators with high OSRs, this has always been true. Pipeline A/D converters rarely see gains much larger than 8 or 16 in the first stage, but even then, this will reduce the noise influence from later stages.

As with the input-referred noise, the disparity in clocking efficiencies between delaying and non-delaying stages is not as significant if the first stage gain is large, resulting in a smaller second stage and therefore a smaller additional load capacitance on the amplifying/integrating phase. This is also why resonator structures in ΔΣ modulators (which require half-delaying integrators [4]) are not detrimental to the total power consumption; these stages are later in the modulator, and with high OSRs they are much smaller.

3.3.3 Anti-Aliasing and Decimation

The anti-aliasing requirements on a pipeline A/D converter and ΔΣ modulator oversampled by the same amount are similar. The anti-aliasing requirements on both architectures are reduced by the OSR since out-of-band signals between $f_s/(2 \cdot OSR)$ and $f_s/2$ can be filtered by the digital decimation filter.

The decimation filter requirements of a high-order ΔΣ modulator are greater than those of the pipeline converter. An 8^{th}-order ΔΣ modulator requires a 9^{th}-order low-pass filter to attenuate the out-of-band noise so that it does not contribute significantly to the in-band noise after downsampling. For the same attenuation of noise before downsampling, an 8-stage pipeline only requires a 1^{st}-order low-pass filter (although a higher order filter is necessary to reduce attenuation at the signal band edge).

The difference in power consumption between the decimation filters in a pipeline converter and a ΔΣ modulator depends on several factors including the target resolution, the technology, and the sampling frequency. In a thermal noise limited design the analog power of the converter increases by 4 times for every added bit. Therefore, at high resolution the digital power should not be a significant fraction of the total power in the converter. However, as the target resolution decreases, the digital power will become more significant in the ΔΣ modulator due to the increased complexity of the decimation filter.

Chapter 4

Incremental Data Converters at Low OSRs

The design of incremental A/D converters at low OSRs are discussed in this chapter. Section 4.1 begins by explaining why incremental A/D converters have higher SQNRs than $\Delta\Sigma$ modulators at low OSRs, and this is followed by discussions surrounding the architectural design issues of cascaded incremental A/D converters. Section 4.2 then explores the advantages of time-interleaving incremental A/D converters, focusing on cascaded architectures. Finally in Section 4.3 the proposed high-speed cascaded incremental A/D converter with an OSR of 3 is presented.

4.1 Operation at Low OSRs

4.1.1 Incremental vs. $\Delta\Sigma$

At low OSRs, incremental data converters have higher SQNRs than $\Delta\Sigma$ modulators. The reason comes from the fact that the two converters operate on different principles, especially at low OSRs where the resetting nature of incremental data converters is more significant. Repeating Eq. 2.17 and Eq. 2.18 for convenience, a single-stage incremental A/D converter has

$$N_{\text{inc,ss}} = \alpha(N-1)\frac{(M+L-1)!}{L!(M-1)!}+1 \tag{4.1}$$

output levels while a cascaded incremental A/D converter has

$$N_{\text{inc,casc}} = \alpha(N-1)^L\frac{(M+L-1)!}{L!(M-1)!}+1 \tag{4.2}$$

output levels for an N-level quantizer, L^{th}-order converter, an OSR of M, and stable input range of α. The contrasting feature of incremental A/D converters when compared to $\Delta\Sigma$ modulators is that for any non-zero value of L, M and N, the number of output levels will be one or more. Unlike $\Delta\Sigma$ modulators at low OSRs where noise-shaping increases the total quantization noise power of the system, incremental A/D converters will always have a minimum resolution equal to the quantizer resolution, even at an OSR of 1 (this OSR will be discussed in Section 4.1.2).

Table 4.1 compares simulated SQNRs of a $\Delta\Sigma$ modulator and an incremental A/D converter at an OSR of 2, 4, 8 and 16 using an NTF of $(1-z^{-1})^2$ with a 2^{nd}-order cascaded architecture (with 3-level quantizers and an interstage gain of 2) as well as a 2^{nd}-order single-stage architecture (with a 5-level quantizer). At a low OSR of 2 and 4, the incremental A/D converter has a larger SQNR, while at an OSR of 8, the results are similar. At higher OSRs of 16 and above, the $\Delta\Sigma$ modulator has a larger SQNR. These results motivate the use of incremental A/D converters instead of $\Delta\Sigma$ modulators at lower OSRs. It can also be seen that cascaded incremental data converters outperform single-stage incremental data converters, as expected according to Eq. 4.1 and Eq. 4.2.

OSR	Incremental Cascaded $N=3/3$	Incremental Single-Stage $N=5$	$\Delta\Sigma$ Cascaded $N=3/3$	$\Delta\Sigma$ Single-Stage $N=5$
2	26 dB	24 dB	17 dB	11 dB
4	35 dB	33 dB	31 dB	25 dB
8	46 dB	44 dB	46 dB	40 dB
16	57 dB	54 dB	59 dB	56 dB

Table 4.1: SQNR Comparison of $\Delta\Sigma$ and incremental A/D converters at low OSRs.

As another example, Fig. 4.1 shows an SQNR comparison at increasing OSRs for an 8^{th}-order cascaded $\Delta\Sigma$ modulator, an 8^{th}-order cascaded incremental A/D converter, and an 8-stage pipeline A/D converter. Each stage has a 3-level quantizer so that the three converters are almost identical architecturally. As long as the OSR is less than 5.3, the incremental A/D converter has a higher SQNR than the other two architectures. Beyond an OSR of 5.3, the noise-shaping in a $\Delta\Sigma$ modulator outperforms incremental A/D conversion. It can also

be seen that a ΔΣ modulator only outperforms a pipeline A/D converter at OSRs greater than 2.5; at lower OSRs ΔΣ modulators increase the total noise power to an extent where it is more beneficial to avoid noise-shaping altogether. This was discussed in Section 3.1.2.

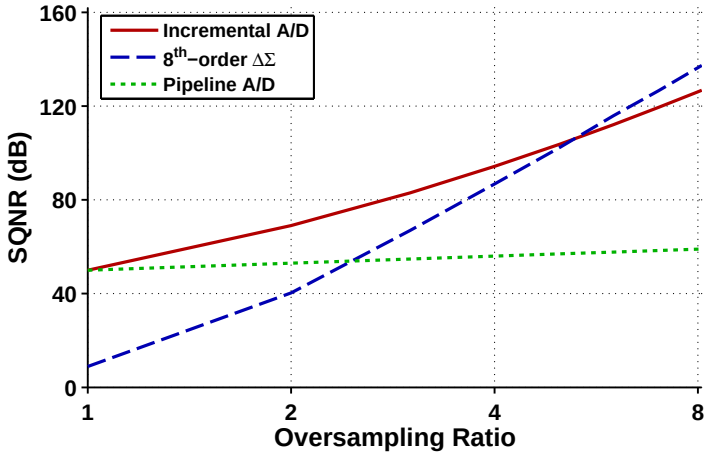


Figure 4.1: Simulated SQNR vs. OSR for 3 different architectures. All three A/D converters have the same internal 3-level quantizers. Simulations for the incremental A/D converter match Eq. 4.2.

Incremental A/D converters and ΔΣ modulators operate on different principles because the loop filter is reset and the input is held in an incremental converter. Since the incremental A/D converter has less noise than a ΔΣ modulator at an OSR of 1 due to the increased noise power from noise-shaping, it should not be surprising that the incremental A/D converter outperforms the ΔΣ modulator up until the OSR where noise-shaping begins to improve the ΔΣ modulator's resolution. Another reason for the increased resolution of an incremental A/D converter at low OSRs (as mentioned in Section 2.2.3) is the larger allowable signal amplitudes. Since an incremental A/D converter resets after OSR clock cycles, the memory of previous conversions is lost, and thus a sustained large signal has only OSR clock cycles to accumulate in the integrator to overload the quantizer. Therefore, while a ΔΣ limits the signal amplitude at low OSRs as it would at high OSRs, an incremental A/D converter at low OSRs allows larger signal amplitudes than at high OSRs since there are fewer cycles for the signal to accumulate. This can contribute a few extra dB of resolution as the OSR is lowered.

At an OSR of 3, these three architectures can also be compared while varying the

number of stages. The results are shown in Fig. 4.2. At this OSR the incremental A/D converter outperforms the ΔΣ modulator and pipeline A/D converter.

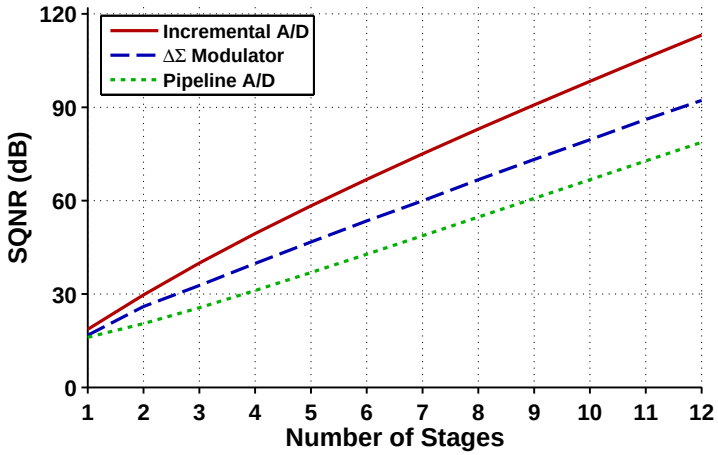


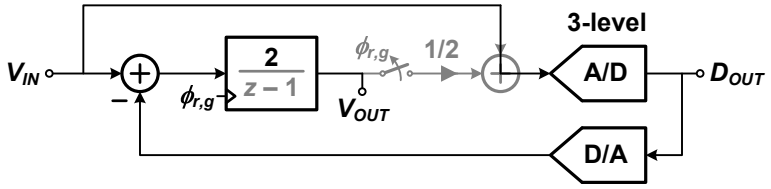
Figure 4.2: Simulated SQNR vs. Number of Stages for 3 different architectures at an OSR of 3 with 3-level internal quantizers. For the incremental converter and ΔΣ modulator, the number of stages is equivalent to its order since they use a cascade of 1^{st}-order stages. Again, simulations for the incremental A/D match Eq. 4.2.

4.1.2 Pipeline Equivalency

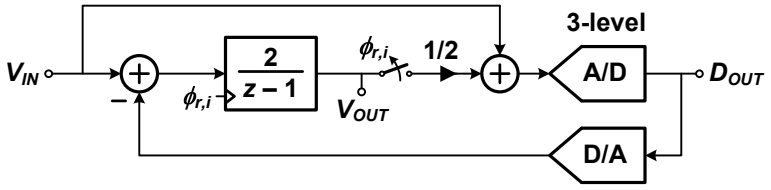
As pointed out in the previous section, even with an OSR of 1, the incremental A/D converter still resolves the input signal with the internal quantizer. If a cascaded incremental A/D converter is used, Eq. 4.2 predicts $\alpha(N-1)^L+1$ output levels for an L^{th}-order converter with N-level quantizers. This is identical to the resolution of an L-stage pipeline A/D converter with N-level internal quantizers and an extra level of redundancy per stage. In fact, when the incremental A/D converter has an OSR of 1, it is effectively a pipeline A/D converter.

More specifically, an input feed-forward cascaded incremental A/D converter can be thought of as a pipeline A/D converter (which already has a S/H) where the OSR determines how frequently resetting is performed. Architecturally the two are almost identical; the main difference is in designing a gain stage or an integrating stage. A single stage of both architectures is shown Fig. 4.3 and they are almost identical. The incremental A/D converter stage uses a resetting integrator while the pipeline A/D converter uses a gain stage

which is effectively an integrator that resets on every clock cycle $\phi_{r,g}$. Also, the addition at the quantizer input in the incremental converter occurs on all clock cycles except for the resetting phase $\phi_{r,i}$. This is also true for the pipeline converter stage, but since it resets on every clock cycle, this addition is never performed.



(a) Resetting Gain Stage



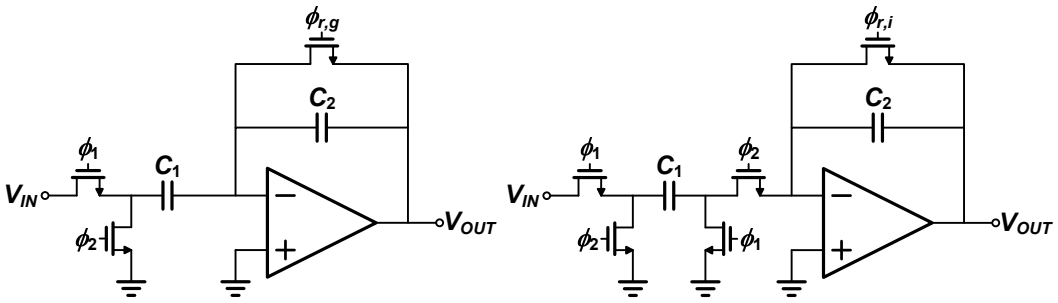
(b) Resetting Integrating Stage

Figure 4.3: The architectural difference between the stages of a pipeline A/D converter and an input feed-forward cascaded incremental A/D converter.

At the circuit level, a resetting gain stage and a resetting integrating stage are shown in Fig. 4.4. The gain stage clock $\phi_{r,g}$ resets on ϕ_1, while the integrator clock $\phi_{r,i}$ resets on ϕ_1, but only every M^{th} clock cycle (for an OSR of M). Aside from a couple switches, the only difference is in the resetting sequence. With the same C_1 and C_2 (a reasonable assumption since C_1 determines the thermal noise, and C_2 controls the gain), both OTAs would be designed almost identically.

4.1.3 Removing the Input S/H

An incremental A/D converter ideally requires an accurate S/H circuit on the input. The design of this block can be difficult, especially when trying to achieve better than 10-bit performance. A S/H circuit also costs extra power since an extra circuit is needed, and this circuit contributes more noise to the entire A/D converter, requiring increased power in the rest of the converter to lower the total noise. Removing the S/H results in a modified



(a) Resetting Gain Stage (b) Resetting Integrating Stage

Figure 4.4: The circuit-level difference between a pipeline A/D converter and an incremental A/D converter lies in the resetting sequence of the gain or integrating stage.

STF which causes some high-frequency attenuation. This can be understood by analyzing a 1st-order converter and extending the result to higher-order converters.

In a single-bit 1st-order incremental A/D converter it will be shown that the output of one conversion will always be the same as long as the average of the input for that conversion is constant (assuming no quantizer overload). For an input V_{IN}, assuming an input feed-forward architecture, the input to the quantizer after the first M clock cycles will be

$$\begin{aligned}
V_Q[1] &= V_{IN}[1] \\
V_Q[2] &= V_{IN}[1] + V_{IN}[2] - V_{REF} \cdot D_1[1] \\
V_Q[3] &= V_{IN}[1] + V_{IN}[2] + V_{IN}[3] - V_{REF} \cdot (D_1[1] + D_1[2]) \\
&\vdots \\
V_Q[M] &= \sum_{i=1}^{M} V_{IN}[i] - \sum_{i=1}^{M-1} V_{REF} \cdot D_1[i].
\end{aligned} \tag{4.3}$$

If it is assumed that the converter is operating within the converter input range where the quantizer is not overloaded, then $-2V_{REF} < V_Q[M] < 2V_{REF}$. Therefore, if the last sample $D_1[M]$ is included in the inequality,

$$-V_{REF} < V_Q[M] - V_{REF} \cdot D_1[M] < V_{REF} \tag{4.4}$$

which is equivalent to

$$-V_{REF} < \sum_{i=1}^{M} V_{IN}[i] - \sum_{i=1}^{M} V_{REF} \cdot D_1[i] < V_{REF}. \tag{4.5}$$

For a given sum of inputs throughout the M cycles $\sum_{i=1}^{M} V_{IN}[i]$, there is a unique sum of digital outputs $D_{OUT} = \sum_{i=1}^{M} D_1[i]$ that will keep Eq. 4.5 bounded within $\pm V_{REF}$. As long as $\sum_{i=1}^{M} V_{IN}[i]$ is constant, D_{OUT} will be constant. Since D_{OUT} is simply the final digital output of the incremental A/D converter after going through the accumulating decimation filter, this will be a unique digital output as long as the sum of the inputs $V_{IN}[i]$ is constant (which is equivalent to keeping the average of the input samples constant).

If the input of the 1st-order incremental A/D converter is averaged and then passed through a S/H, this system will be identical to one where a moving input enters the system with no S/H since the output is only a function of the sum. For example, if three samples of a moving input 0.1, 0.2, and 0.3 enter the first integrator of the system (for an OSR of 3), it is identical to a held input of 0.2 entering the first integrator for three cycles. So the incremental A/D converter with a moving input can be modeled as a typical incremental A/D converter where the S/H is preceded by an averaging filter $G(z)$, as shown in Fig. 4.5. This provides a direct way to analyze the effect of the moving input on an incremental A/D converter using the filter $G(z)$.

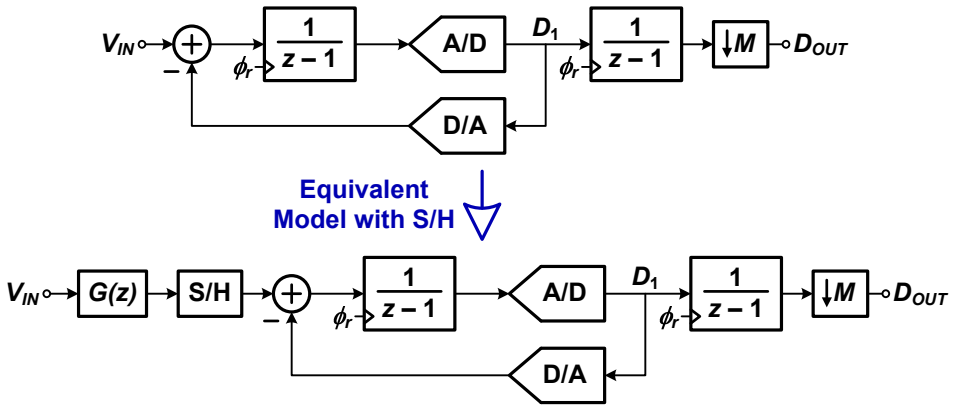


Figure 4.5: Model of an incremental A/D converter with no S/H, and its equivalent model with an input S/H. $G(z)$ is not explicitly used, but it is the effective modification of the STF when the S/H is removed.

The filter $G(z)$, while not explicitly present in the incremental A/D converter, effec-

tively modifies the STF when the input S/H is removed. Depending on the modulator order, $G(z)$ will have a different shape. The filter is of the form [70]

$$G(z) = \frac{1 + z^{-1} + z^{-2} + ... + z^{-(M-1)}}{M} \tag{4.6}$$

for a 1st-order incremental with an OSR of M. Fig. 4.6 shows $G(z)$ with an OSR of 3. Since the input signal is limited to $f_s/(2 \cdot OSR)$, the attenuation will be no larger than 3.52 dB at the signal band edge, represented by the vertical dotted line in Fig. 4.6. The filter is a digital sinc filter similar to what was seen in the dual-slope A/D converter (which inherently had no S/H). While input signals between $f_s/(2 \cdot OSR)$ and $f_s/2$ will still alias back into the signal band, they will be attenuated according to the STF.

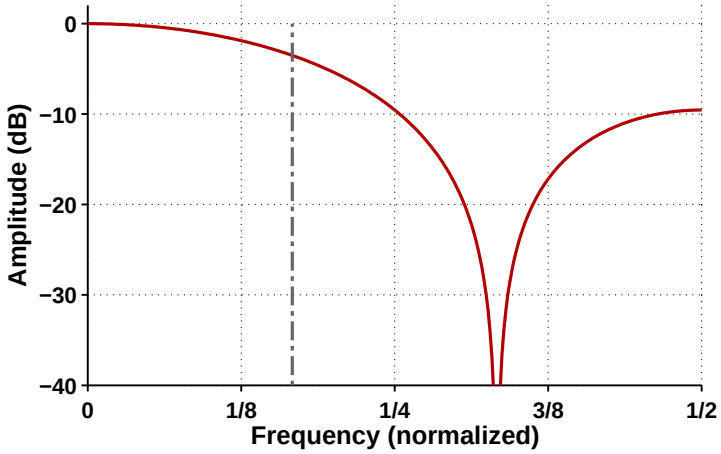


Figure 4.6: $G(z)$ for a 1st-order incremental A/D converter with an OSR of 3.

The discussion can be extended to find STFs of higher-order converters with removed S/H blocks. For these architectures the STF is a weighted sum of inputs $V_{IN}[i]$ that are held constant, resulting in a more complicated filter $G(z)$ that is a weighted average of the inputs. The resulting equivalent filter $G(z)$ for a 2nd-order incremental A/D converter with a moving input is

$$G(z) = \frac{1 + 2z^{-1} + 3z^{-2} + ... + Mz^{-(M-1)}}{M \cdot (M+1)/2}. \tag{4.7}$$

The STF of this incremental A/D converter for an OSR of 3 is shown in Fig. 4.7. The

attenuation is 2.78 dB at the signal band edge. The attenuation at the signal band edge is less and will continue to reduce for higher-order incremental A/D converters with the input S/H removed. Generalizing to an L^{th}-order converter (assuming an L^{th}-order accumulating decimation filter equal to the NTF), the STF is

$$G(z) = \frac{1 + \ldots + \frac{(M-2+L-1)!}{(M-2)!(L-1)!} z^{-(M-2)} + \frac{(M-1+L-1)!}{(M-1)!(L-1)!} z^{-(M-1)}}{\frac{(M+L-1)!}{M!(L-1)!}}. \tag{4.8}$$

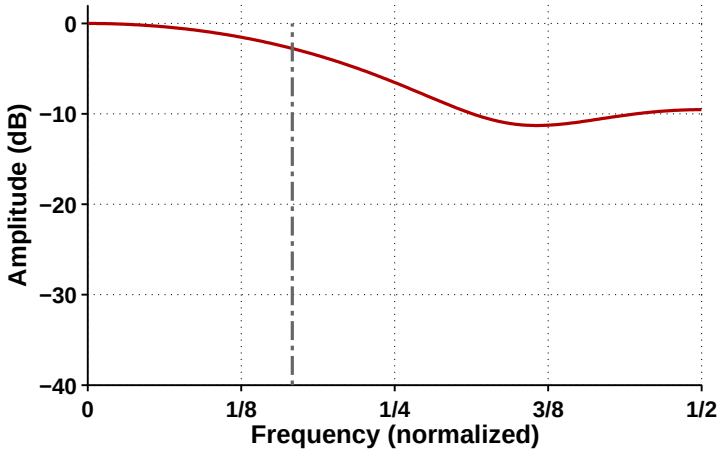


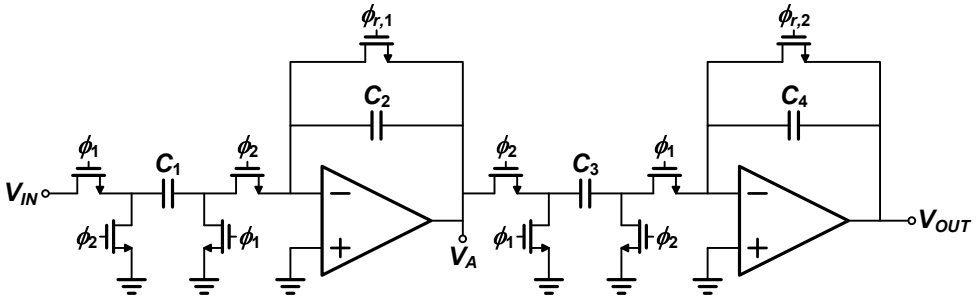
Figure 4.7: $G(z)$ for a 2^{nd}-order incremental A/D converter with an OSR of 3.

To maintain a unity-gain in the signal band an additional digital filter can be added which is equal to the inverse of $G(z)$ throughout the signal band. This increases the quantization or thermal noise towards the signal band edge but the overall increase in noise is small since the majority of the noise is at lower frequencies and does not get amplified. For example, with the 1^{st}-order converter of Fig. 4.6 at an OSR of 3 the noise increases by only 1.05 dB, and this will be less for higher-order converters.

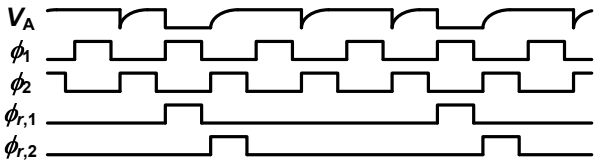
4.1.4 Resetting Efficiency

One difficulty in designing power efficient incremental A/D converters at low OSRs is the reset phase. The simple way to reset the converter is to do the same as is done in a pipeline A/D converter. If each stage is delayed by half a clock cycle (i.e., odd stages are sampled

on ϕ_1 and even stages are sampled on ϕ_2), then half a clock cycle is available to reset the integrator. As shown in Fig. 4.8, the first stage input is sampled on ϕ_1 and integrated on ϕ_2 and the opposite clock phases are used for the second stage. For an OSR of M, on every M^{th} clock phase of ϕ_1 the integrator is reset by $\phi_{r,1}$, and the entire ϕ_1 clock phase is available to reset. Because the first integrator output will only be valid at the end of ϕ_2 (due to the occasional reset during ϕ_1), the second integrator must sample on ϕ_2. The corresponding reset switch $\phi_{r,2}$ will then reset on every M^{th} clock phase of ϕ_2.



(a) Resetting Integrator



(b) Clocking (OSR of 3)

Figure 4.8: Resetting scheme for two cascaded integrators in an incremental A/D converter.

The resetting scheme of Fig. 4.8 is power inefficient because when the subsequent stage has a similarly sized capacitor as the current stage, additional loading occurs during the amplifying/integrating phase which is the phase that typically limits the OTA bandwidth. To charge the subsequent stage's sampling capacitance extra current must be drawn from the amplifier. This results in a larger amplifier and a reduced feedback factor β, further increasing the amplifier size. This is the same inefficiency discussed in Section 3.3.2.

At low OSRs, C_3 will likely be a significant fraction of C_2 and this increased load on the first integrator stage will increase the OTA size. An overdesign is required in the amplifying/integrating phase while in the sampling phase the OTA simply holds the current value and any power dissipated is wasted (although it cannot be turned off since it needs to hold

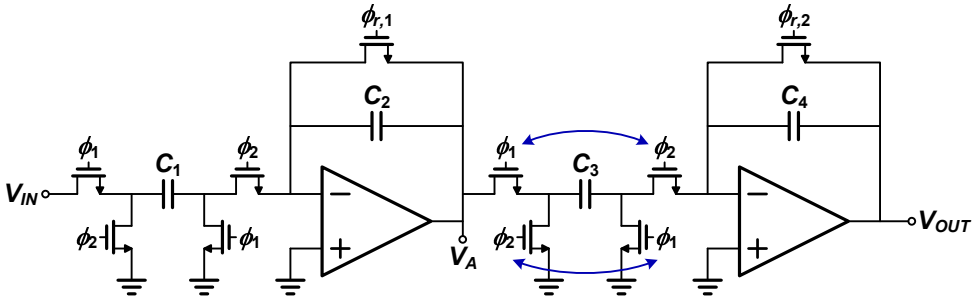
the value on the capacitor). This is wasteful since both phases have different requirements on the current consumption; it is far more efficient when the requirements on both phases are almost identical. The specific efficiencies are dependent on the architecture and the number of quantizer levels, but using half-delaying stages has the potential to increase the power by more than a factor of 2.

As an example, if the second stage is designed to contribute half the input-referred noise power of the first stage at an OSR of 3, then the second stage would be designed about 3 times smaller and $C_3 = C_1/3$. Also, if the first stage integrator coefficient is 2, then $C_1 = 2C_2$. When the first stage is not loaded by the second stage, the OTA sees a feedback capacitance of $2C_2/3$. When it is loaded by the second stage, the sampling capacitance of the second stage $C_3 = 2C_2/3$ is added to the feedback capacitance, resulting in a doubling of the total capacitance seen by the first stage OTA, and hence a doubling of the OTA power.

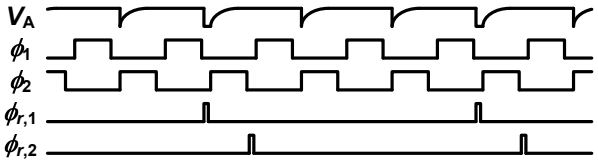
Fully-delaying stages where the subsequent stage is sampled on the same clock phase as the current stage will reduce the load capacitance on the first OTA, resulting in a power savings. However, the resetting becomes more difficult; the integrator output has to be valid during ϕ_1 to pass to the next stage, but it is on ϕ_2 that the sampled signal is integrated. So on both clock phases the integrator is being used and neither of the clock phases are available for resetting. This leaves the non-overlap time for the resetting phase, as shown in Fig. 4.9.

Resetting in the non-overlap time is difficult at high clock speeds. If the non-overlap time of a two-phase clock is a few hundred picoseconds, then the switch sizes to fully discharge (to 10-bit resolution) a capacitor of a few picofarads could be several hundred microns (this depends on several factors such as common-mode voltages, power supply, choice of *n-channel metal-oxide-semiconductor* (NMOS) or *p-channel metal-oxide-semiconductor* (PMOS) switches, etc.). Due to the unreasonably large switches that will introduce charge injection errors of their own, another alternative exists.

Instead of trying to reset in the non-overlap time, one capacitor can be switched out of the circuit while a new one is switched in, and while the capacitor is switched out and not being used it can be reset. During that time, the new capacitor can be used in the integrator for the next M clock cycles, after which it will be switched out and the newly reset capacitor can be switched back in. This is shown in Fig. 4.10 where $C_{2\mathrm{o}}$ and $C_{4\mathrm{o}}$ are used for integration on the odd clock phases, and $C_{2\mathrm{e}}$ and $C_{4\mathrm{e}}$ are used for integration on the even clock phases.



(a) Modified Resetting Integrator



(b) Modified Clocking (OSR of 3)

Figure 4.9: Modified fully-delaying resetting scheme for two cascaded integrators in an incremental A/D converter.

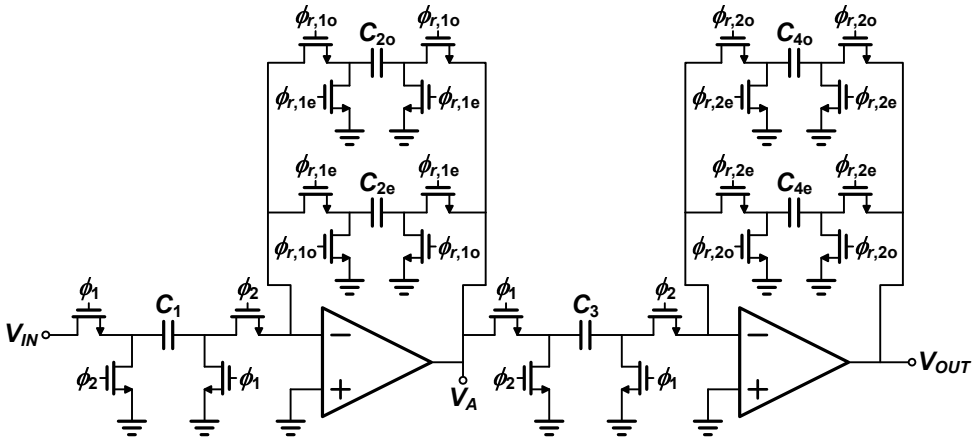
The disadvantage with this two-phase clocking scheme is that twice as many capacitors are necessary, adding to the silicon area. Also, the two capacitors have to be well matched, otherwise the odd and even output samples will have different gains. However, if such a mismatch exists, it can be calibrated in the same way that gain errors are calibrated where two algorithms would need to independently operate on opposing samples to equalize the different gains.

4.2 Time-Interleaved Incremental A/D Converters

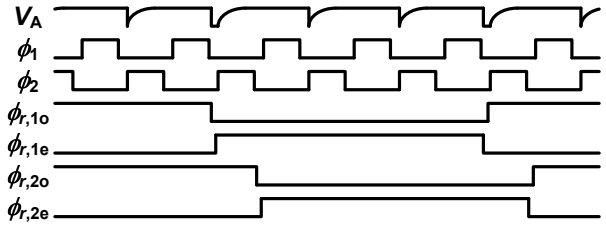
4.2.1 Time-Interleaving

Incremental A/D converters can be time-interleaved by placing n incremental converters in parallel, resulting in an effective sampling frequency of $n \cdot f_s$ [51]. Alternatively, for an OSR of M, this can be viewed as effectively reducing the OSR to M/n, resulting in an increase in the signal bandwidth by n.

The clocking scheme of a time-interleaved incremental A/D converter is modified so that each parallel branch resets one phase after the reset of the preceding branch, while



(a) Two-Phase Resetting Integrator

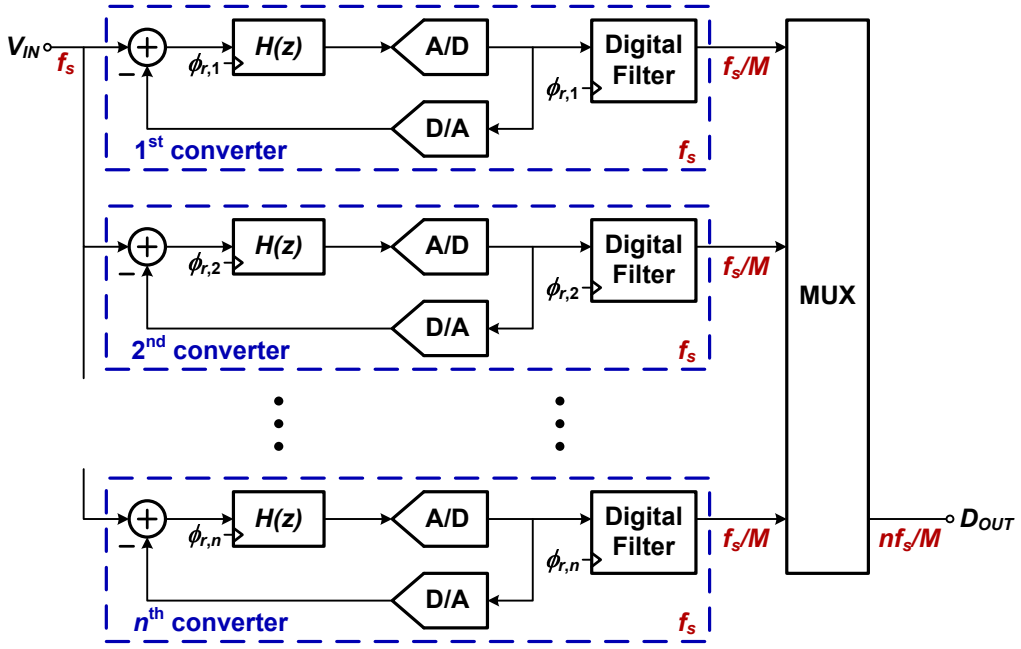


(b) Two-Phase Clocking (OSR of 3)

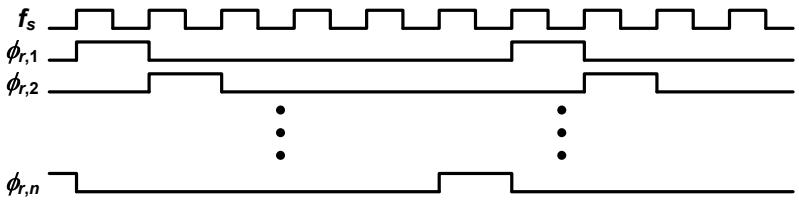
Figure 4.10: Fully-delaying two-phase resetting scheme for two cascaded integrators in an incremental A/D converter.

the input feeds all branches identically. This is shown in Fig. 4.11 (an alternative time-interleaving scheme is discussed in Appendix C). At first it might seem unusual that the input samples to each parallel branch are identical. However, with no S/H the first samples of each parallel branch are dependent on the resetting scheme of their respective branch, and each branch sees a different first sample.

Time-interleaved incremental A/D converters have several advantages. First, contrary to time-interleaved $\Delta\Sigma$ modulators, all the circuitry is operating at the sampling rate or slower since it does not require higher-rate multiplexing at the input, or higher-rate down-sampling at the output, reducing the digital power of the decimator. Also, there is no cross-coupling between the parallel branches so there is no critical path to overcome [57]. Lastly, no input signal images occur in the output spectrum [59]. These advantages lead to an important result; the time-interleaved incremental A/D converter can be time-interleaved



(a) Architecture



(b) Clocking

Figure 4.11: Time-interleaved incremental A/D converter. The clocking scheme is such that each individual converter resets in sequence.

by the same amount that it is oversampled, resulting in a modulator that oversamples data in each parallel branch (thus reducing the requirements on the DC gain, linearity, etc.) while still attaining the speed of a Nyquist-rate A/D converter. The challenge is in choosing a modulator where the STF minimally attenuates the signal at input frequencies near $f_s/2$.

4.2.2 Signal Transfer Function

Since no S/H is used on the input of the time-interleaved incremental A/D converter, input signal attenuation results at higher input frequencies. The STFs for 1st- and 4th-order in-

cremental A/D converters with OSRs of 4 are shown in Fig. 4.12. The STFs for the same incremental A/D converters are shown in Fig. 4.13 with OSRs of 8. From these plots it is clear that increased high-frequency attenuation is seen in the STF of the lower-order modulator, as well as at the higher OSR. Despite these trends, none of these STFs would be appropriate when trying to time-interleave incremental A/D converters and resolve the full signal bandwidth of $f_s/2$.

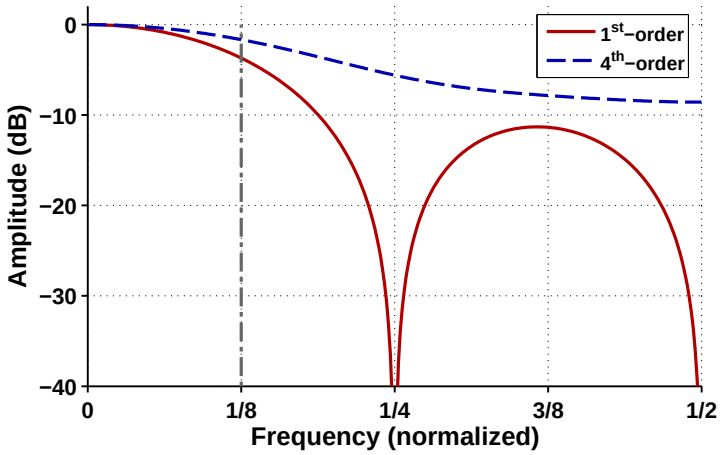


Figure 4.12: STF for a 1st- and 4th-order incremental A/D converter with an OSR of 4.

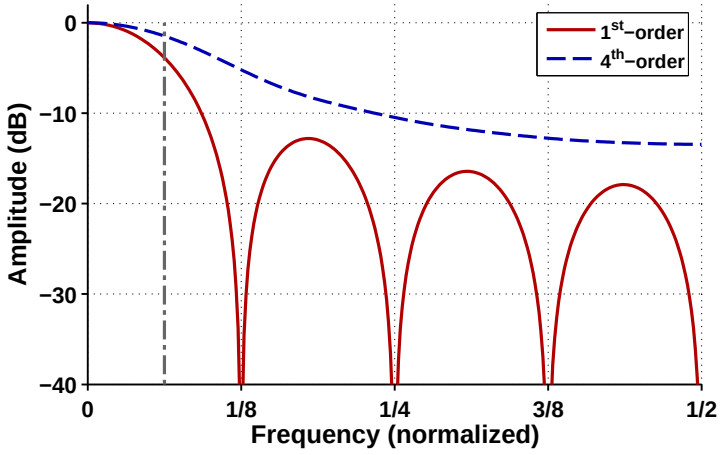


Figure 4.13: STF for a 1st- and 4th-order incremental A/D converter with an OSR of 8.

The STF degradation improves for higher-order modulators since the first input sample has a higher weighting towards the final output, thus making the output primarily dependent on the first sample, and less dependent on the other samples (at the expense of increased input-referred noise, as mentioned in Section 2.2.4). One method to reduce the STF attenuation is to sample the input twice, so that the first two samples are based on the same input (like a two-sample S/H). Referring to Eq. 4.8, this effectively sums the coefficient of the odd terms with the coefficients of the adjacent even terms while eliminating the even terms. As an example, the STF of a 4^{th}-order converter with an OSR of 4 is

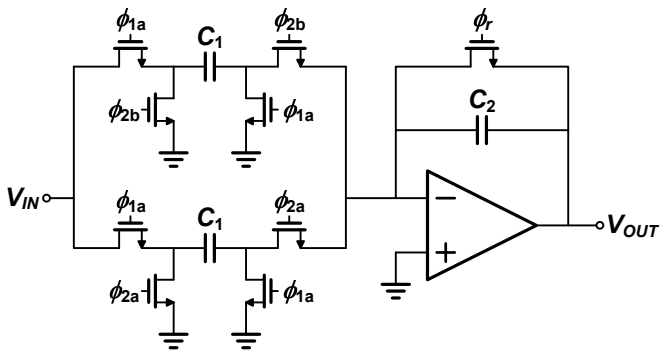
$$G(z) = \frac{1 + 4z^{-1} + 10z^{-2} + 20z^{-3}}{35} \tag{4.9}$$

while the STF of a 4^{th}-order converter with an OSR of 4 and a double-sampled input is

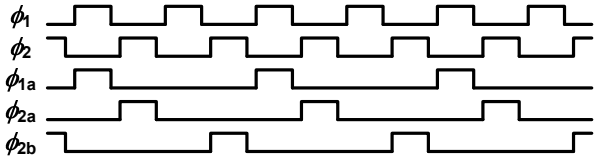
$$G(z) = \frac{(1+4) + (10+20)z^{-2}}{35}. \tag{4.10}$$

Fig. 4.14 illustrates the proposed double-sampled switching scheme for a first-stage integrator. The resulting STFs of the incremental A/D converters with OSRs of 4 are shown in Fig. 4.15. With the double-sampling technique it can be seen that the high-frequency attenuation is far less than in the original STFs of Fig. 4.12.

This technique could be extended to sample the input more than twice, but there are a couple of drawbacks which limit the number of input samples that could be sampled at one time. The silicon area is increased since there are two paths to perform the sampling operation, resulting in twice the capacitance. Also, a more complicated (lower-speed) clocking scheme is required. Matching between the two (or more) capacitors, however, is not a problem since it only affects the magnitude of the input signal entering the modulator. It should be noted that if this scheme is used for a time-interleaved incremental A/D converter, it does not increase the loading on the circuitry that drives the first stage since the total load capacitance evens out across all the parallel stages. When the input is sampled twice by the first parallel branch, adding a load capacitance of $2 \cdot C_1$, it will not be sampled by the next parallel branch, so the average load capacitance C_1 per parallel stage is maintained on every sample. This would not be the case if this technique were used on a regular incremental A/D converter, therefore it is only mentioned as an improvement for the time-interleaved converter.



(a) Switched-Capacitor Circuit



(b) Clocking Scheme

Figure 4.14: Proposed double-sampled switching scheme. The clock ϕ_{1a} samples the input twice on every second ϕ_1, while clock ϕ_2 is divided into ϕ_{2a} and ϕ_{2b}.

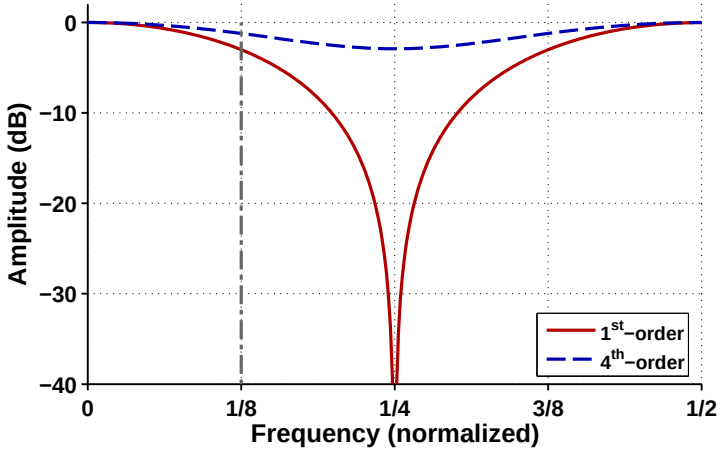


Figure 4.15: Double-sampled STF for a 1st- and 4th-order incremental A/D converter with an OSR of 4.

Extending the double-sampling technique to an OSR of 8 where the input is quadruple-sampled, the STFs of the incremental A/D converters with an OSR of 8 are shown in Fig. 4.16. The quadruple-sampling technique on an incremental converter with an OSR

of 8 has a similar effect as the double-sampling technique on a converter with an OSR of 4; this is most apparent in the 1^{st}-order converter where half the spectral nulls are eliminated. If quadruple-sampling were used on a converter with an OSR of 4, the STF would be unity across all frequencies.

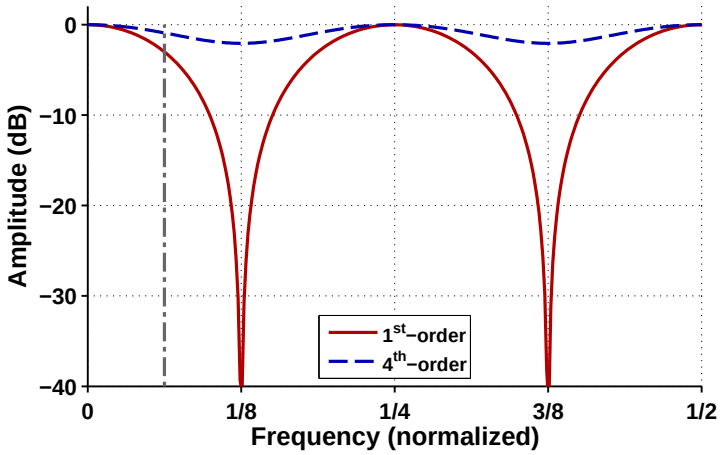


Figure 4.16: Double-sampled STF for a 1^{st}- and 4^{th}-order incremental A/D converter with an OSR of 8.

4.2.3 Matching and Calibration

One major concern when time-interleaving A/D converters is matching between paths. The required matching accuracy is similar to the modulator resolution. This is the same constraint that is imposed on the analog circuitry of a cascaded incremental A/D converter where the DC gain and linearity must all be at the modulator resolution since the analog filters must match the digital filters (see Appendix B). Therefore, if a cascaded architecture is used for the incremental A/D converter, then time-interleaving does not impose a significant difference in the required circuit performance.

The circuit performance requirements of a cascaded incremental A/D converter are quite stringent when high resolution is desired, and calibration may be needed to achieve the full resolution. Similar to a cascaded $\Delta\Sigma$ modulator, the analog filters must match the digital filters to avoid any noise leakage from earlier stages to the output. Some of the techniques presented in [44, 71] for calibrating cascaded $\Delta\Sigma$ modulators can be applied

to incremental A/D converters to match the back-end digital filter to the non-ideal analog filters.

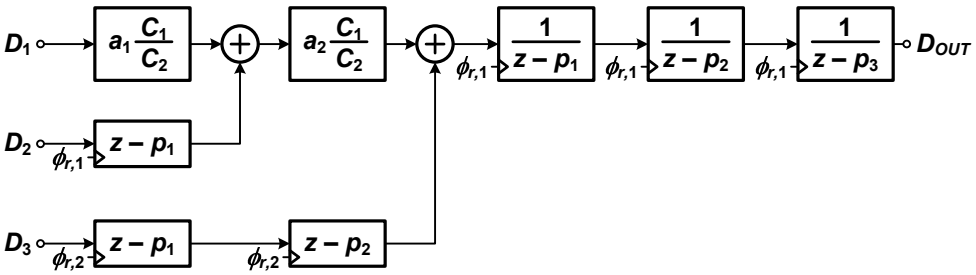


Figure 4.17: Digital calibrating filter for a cascaded incremental A/D converter. A 3rd-order structure is shown for simplicity, but it can be easily extended to an L^{th}-order modulator where L digital paths combine to a final D_{OUT}.

The coefficients that need calibrating in an incremental A/D converter are similar to those of a cascaded $\Delta\Sigma$ modulator. A non-ideal integrator can be modeled as [4]

$$I(z) = \frac{C_1}{C_2}\frac{a}{z-p} \tag{4.11}$$

where a and p are functions of the capacitor ratio C_1/C_2 and finite DC gain A according to the following equations:

$$a = \frac{1}{1+(1+C_1/C_2)/A} \tag{4.12}$$

$$p = \frac{1+1/A}{1+(1+C_1/C_2)/A}. \tag{4.13}$$

If the cascaded incremental A/D converter is an ideal cascade of 1st-order modulators, then the back-end digital filter is as shown in Fig. 4.17 where the differentiators and accumulators are reset on the appropriate phases, and all the a_i and p_i coefficients are unity. If the integrators are non-ideal so that the coefficients $\{a_i, p_i\}$ characterize the i^{th} 1st-order modulator (according to Eq. 4.11), then the back-end digital filter shown in Fig. 4.17 will perfectly calibrate the incremental A/D converter. No noise leakage will occur when the modulator is perfectly calibrated so that the only remaining quantization noise error term will exist from the quantization in the last stage. For an L^{th}-order cascade of 1st-order modulators oversampled by 4 with an input V_{IN} and an L^{th}-stage quantization error ε_L, the

output D_{OUT} is equal to (assuming a slowly varying input signal for simplicity)

$$D_{OUT} = K_1 V_{IN} + K_2 \varepsilon_L \tag{4.14}$$

where

$$K_1 = \prod_{i=1}^{L-1} a_i \Big(1 + \sum_{i=1}^{L} p_i + \sum_{i=1}^{L} \sum_{j=i}^{L} p_i p_j + \sum_{i=1}^{L} \sum_{j=i}^{L} \sum_{k=j}^{L} p_i p_j p_k \Big) \tag{4.15}$$

and

$$K_2 = 1 + (a_L - p_L) + (a_L - p_L)^2 + (a_L - p_L)^3. \tag{4.16}$$

The coefficient K_2 does not deviate much from unity since both a_L and p_L are close to unity (note that a_L and p_L are defined as in Eq. 4.12 and Eq. 4.13 for the L^{th}-stage of the converter). The only drawback is that the product of the coefficients for K_1 can reduce the signal amplitude slightly. For example, in an 8^{th}-order modulator with integrator DC gains of 40 dB, the signal will be attenuated by 2.25 dB.

4.3 Proposed High-Order Incremental A/D Converter

4.3.1 Architecture

As has been discussed, high-order cascaded architectures are better suited to low OSR incremental A/D designs. The chosen architecture, shown in Fig. 4.18, is an 8^{th}-order cascade of 1^{st}-order stages with 3-level quantizers and an OSR of 3. Each individual stage has an input feed-forward path and an NTF of $(1 - z^{-1})$. With the input S/H removed, the STF of the proposed architecture is shown in Fig. 4.19. The attenuation is 0.97 dB at the signal band edge. This is relatively small and would likely be considered a worthwhile trade-off since the high power S/H is no longer needed.

A sample plot of the downsampled spectrum is shown in Fig. 4.20. It has a peak SQNR of 83.5 dB, 9.5 dB above the intended 74 dB resolution for a 12-bit resolution converter (and 17 dB above the SQNR of the equivalent $\Delta\Sigma$ modulator). The increased input noise due to the uneven weighting of the input samples is 3.05 dB. The corresponding weighting parameters for the architecture are $w_i = \{1/45, 8/45, 36/45\}$.

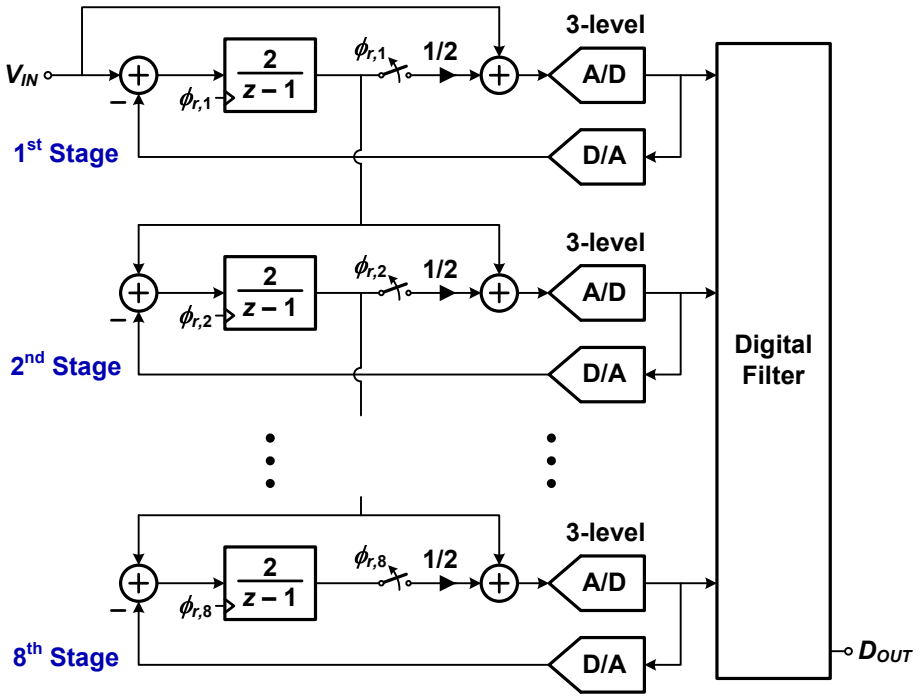


Figure 4.18: Proposed incremental A/D architecture. Each stage is designed identically as a 1st-order input feed-forward stage with a 3-level quantizer.

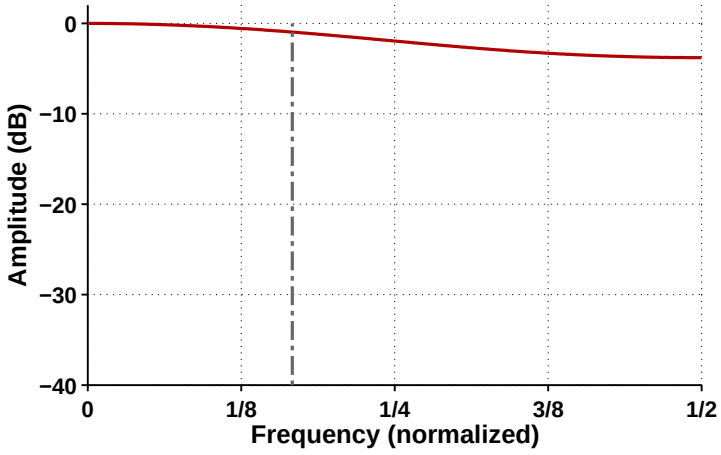


Figure 4.19: STF for an 8th-order incremental A/D converter with an OSR of 3.

4.3.2 Power and Design Comparisons

As was discussed is Section 4.1.2, the cascaded input feed-forward architecture is similar to an oversampled pipline A/D converter. The power of the two can be compared for similar

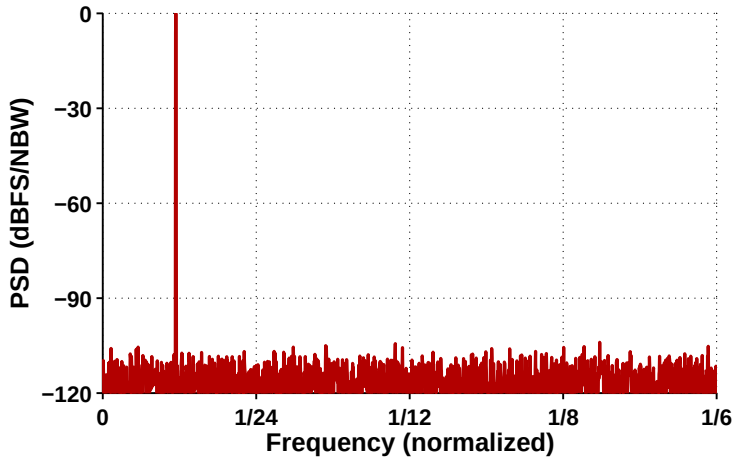


Figure 4.20: Output spectrum for an 8$^{\text{th}}$-order incremental A/D converter (NBW $= 1.2 \times 10^{-4}$).

12-bit architectures.

Input-Referred Noise of a 13-Stage Pipeline

A 1.5-bit/stage pipeline A/D converter requires 13 stages for 12-bit resolution (with 6 dB SQNR margin). If the first stage noise power is normalized to 1, then if each subsequent stage is sized at half the size of the previous stage, then they will contribute $1/2^{n-1}$ to the normalized noise power for the n^{th} stage. This is because the noise input-referred from each stage to the previous stage is decreased by 4 due to the voltage gain of 2 between the stages. For 13 stages, this results in a total normalized noise power of 2.00. If it is assumed that the first stage power is P_1, then the total power will be $2 \cdot P_1$.

Due to practical limitations, it is unreasonable to assume that stages can be continually sized smaller. If it is assumed that the smallest stage will be 8 times smaller than the first stage, then the 4$^{\text{th}}$ to 13$^{\text{th}}$ stage will all be the same size. The total normalized noise power is 1.92 while the total power is $3 \cdot P_1$.

Input-Referred Noise of an 8$^{\text{th}}$-order Incremental

An incremental A/D converter requires 8 stages for 12-bit resolution, leaving a 9 dB SQNR margin. Finding the input-referred noise is more complicated than for a pipeline A/D con-

verter since the gain of each stage is not simply 2.

At an OSR of 3, the time-domain behaviour of the incremental converter can be analyzed for 3 time steps. For a 1st-order converter, after 3 time steps, the downsampled digital output is

$$D_{OUT} \cdot V_{REF} = V_{IN}[1] + V_{IN}[2] + V_{IN}[3] + N_1[1] + N_1[2] + N_1[3] + E_1[3] \tag{4.17}$$

where $V_{IN}[i]$ is the input, $N_n[i]$ is the input noise, and $E_n[i]$ is the quantizer noise at the i^{th} time instant from the n^{th} stage. In this example the total noise power is three times less than with an OSR of 1 since $N_1[1]+N_1[2]+N_1[3]$ is uncorrelated while $V_{IN}[1]+V_{IN}[2]+V_{IN}[3]$ is correlated.

For a 2nd-order converter, after 3 time steps, the downsampled digital output is

$$\begin{aligned} D_{OUT} \cdot V_{REF} = {} & 3V_{IN}[1] + 2V_{IN}[2] + V_{IN}[3] + 3N_1[1] + 2N_1[2] + N_1[3] \\ & + (N_2[1] + N_2[2] + N_2[3] + E_2[3])/2. \end{aligned} \tag{4.18}$$

In this example the total noise power from the first stage is 2.57 times less than with an OSR of 1. This is less than the expected 3 due to the weighting factors on the coefficients of the noise terms N_1. The total noise power from the second stage is 48 times less; a factor of 3 comes from the OSR, but the other factor of 16 reduces the input-referred noise from the second stage by 4 times the factor for the equivalent pipeline converter.

Extending this analysis to an 8th-order converter, the downsampled digital output is

$$\begin{aligned} D_{OUT} = {} & 36V_{IN}[1] + 8V_{IN}[2] + V_{IN}[3] + 36N_1[1] + 8N_1[2] + N_1[3] \\ & + (28N_2[1] + 7N_2[2] + N_2[3])/2 \\ & + (21N_3[1] + 6N_3[2] + N_3[3])/4 \\ & + (15N_4[1] + 5N_4[2] + N_4[3])/8 \\ & + (10N_5[1] + 4N_5[2] + N_5[3])/16 \\ & + (6N_6[1] + 3N_6[2] + N_6[3])/32 \\ & + (3N_7[1] + 2N_7[2] + N_7[3])/64 \\ & + (N_8[1] + N_8[2] + N_8[3] + E_8[3])/128. \end{aligned} \tag{4.19}$$

The input-referred noise from each stage is summarized in Table 4.2. Included is a comparison with an oversampled pipeline A/D converter. Because of the weighting factors, the incremental A/D converter has more input-referred noise from earlier stages, but since the input-referred factor is larger, eventually later stages in the incremental converter contribute less noise than later stages in a pipeline converter.

Stage	Input-Referred Noise Power	
	Incremental A/D	Pipeline A/D
1	1/1.49	1/3
2	1/6.53	1/12
3	1/45.6	1/48
4	1/347	1/192
5	1/2978	1/768
6	1/30297	1/3072
7	1/398190	1/12288
8	1/7432875	1/49152

Table 4.2: Input-referred noise power for each stage of an 8^{th}-order incremental A/D converter with an OSR of 3, and 8 stages of a pipeline A/D converter with an OSR of 3.

If the incremental A/D converter is designed so that each stage is half the size of the previous stage, the total normalized noise power will be 3.29 (factoring out the OSR to directly compare this to the pipeline converter). Since this is larger than for the pipeline converter, the first stage would need to be sized 1.64 times larger, consuming a first stage power of $1.64 \cdot P_1$. Adding in the 7 other stages, the total converter power will be $3.27 \cdot P_1$.

In the more practical case where the later stages are no more than 8 times smaller than the first stage, then the 4^{th} to 8^{th} stage will all be the same size. The total normalized noise power is 3.28, and equalizing this noise to the noise in the pipeline A/D converter results in a total power of $4.06 \cdot P_1$, about 35% more than an equivalent pipeline A/D converter. Despite the improved SQNR, the incremental converter is less power efficient than an equivalent pipeline A/D converter due to the additional noise from the uneven weighting of the input samples (as shown Table 2.1). The thermal noise can be improved depending on the choice

of OSR and order, but this also becomes a trade-off with SQNR. This may limit the low OSR incremental data converter to applications which are not thermal noise limited (for example, matching or flicker noise limited).

4.3.3 Anti-Aliasing and Decimation

The anti-aliasing requirements on an incremental A/D converter are more constraining than those of a pipeline A/D converter. Signals between $f_s/(2 \cdot OSR)$ and $f_s/2$ will alias back into the signal band, resulting in no oversampling advantage in the anti-aliasing filter of an incremental A/D converter.

The decimation filter of an incremental A/D converter is much simpler than that of a pipeline A/D converter since the recombined outputs are simply accumulated by L accumulators (for an L^{th}-order converter) and downsampled, without needing an additional low-pass digital filter to keep out-of-band noise from aliasing back in-band. Conversely, a pipeline converter needs a digital filter to attenuate noise from $f_s/(2 \cdot OSR)$ to $f_s/2$ before the downsampler, and this filter must be designed with a sufficiently sharp cut-off so as not to reduce the usable signal bandwidth. Table 4.3 summarizes the requirements on the anti-aliasing filter and decimation filter for an 8^{th}-order incremental A/D converter and an 8-stage pipeline A/D converter (an 8^{th}-order $\Delta\Sigma$ modulator is also included).

Oversampled Architecture	Anti-Aliasing Filter	Decimation Filter
Incremental Converter	No improvement	No additional digital filtering
Pipeline Converter	Reduced by OSR	Low-pass filter required
$\Delta\Sigma$ Modulator	Reduced by OSR	High-order low-pass filter required

Table 4.3: Comparison of anti-aliasing and decimation filters for an 8^{th}-order incremental A/D converter, an 8-stage pipeline converter, and an 8^{th}-order $\Delta\Sigma$ modulator.

Chapter 5

Circuit Design

This chapter discusses the circuit design for a prototype chip that was fabricated in 0.18 µm CMOS technology. This includes a detailed explanation of the circuits used for the incremental data converter, as well as some transistor-level simulation results.

5.1 A/D System

5.1.1 Architecture

The incremental A/D converter designed is shown in Fig. 5.1. It is an 8^{th}-order cascade of 1^{st}-order stages with 3-level quantizers. The raw data is output from the chip and the digital decimation filter is implemented with Matlab code. As was mentioned in previous sections, a pipeline A/D converter, an incremental A/D converter, and a cascaded incremental A/D converter are similar architecturally and can all be implemented by adjusting the resetting clocks $\phi_{r,1}, \phi_{r,2}, \ldots, \phi_{r,8}$ of Fig. 5.1. The cascaded incremental A/D converter is designed to have controllable OSRs by adjusting the resetting clocks. The three distinct architectures are available by adjusting the incremental data converter to an OSR of 1, 3, and infinity (no resetting).

When the OSR is set to 1 the data converter becomes an 8-stage pipeline A/D converter with 1.5 bits/stage, resulting in an 8-bit converter. Since the integrators are reset on every clock cycle, they act like gain stages instead of integrators. The feed-forward summers of Fig. 5.1 are no longer needed since the path from the integrator/gain stage is always

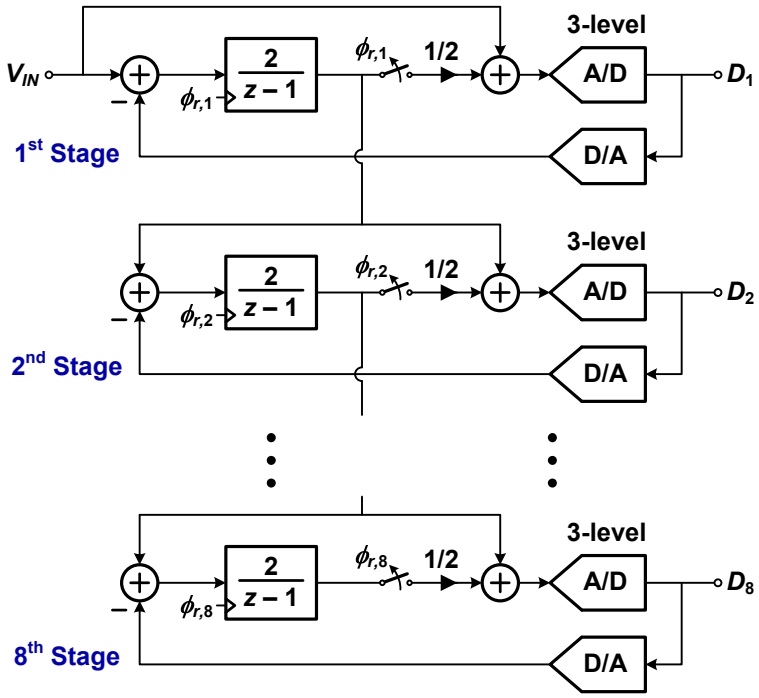


Figure 5.1: A/D converter architecture. Each stage is designed identically as a 1st-order input feed-forward stage with a 3-level quantizer. The reset clock of each stage is adjusted according to the desired A/D converter architecture.

disconnected from it.

When the OSR is set to 3 the data converter becomes an 8-stage incremental A/D converter. The clock phases $\phi_{r,1}$, $\phi_{r,4}$ and $\phi_{r,7}$ are the same; clock phases $\phi_{r,2}$, $\phi_{r,5}$ and $\phi_{r,8}$ are the same; and clock phases $\phi_{r,3}$ and $\phi_{r,6}$ are the same. This architecture was discussed in detail in Section 4.3.

When the OSR is set to infinity (note that setting the OSR to infinity simply refers to the frequency of resetting for the incremental A/D converter) the integrators are never reset and the connection from the integrator to the summer is never removed. The converter becomes an 8^{th}-order cascaded $\Delta\Sigma$ modulator. The analog circuitry remains the same but the decimation filter needs to be modified depending on the intended OSR of the $\Delta\Sigma$ modulator (any OSR can be chosen since the NTF zeros are not optimized). This architecture was discussed in Section 3.3.

The SQNR for these three configurations was shown in Fig. 4.1. The chosen architec-

ture can be reconfigured to realize almost any of the SQNR values on the plot by simply adjusting the resetting scheme and the off-chip decimation filter.

5.1.2 Target Specifications

While most of the SQNR values in Fig. 4.1 can be realized, the noise floor needs to be placed at a specific value. The target resolution for the incremental A/D converter with an OSR of 3 is 69 dB (slightly larger than 11-bits). For both the pipeline and ΔΣ mode (assuming an OSR larger than 3), this results in an overdesign of the thermal noise floor. The circuit design in the next section will be primarily focused on the incremental converter since this architecture requires the highest resolution.

The target sampling frequency is 100 MHz, resulting in a signal bandwidth of 16.7 MHz, with a target power consumption of about 100 mW with a 1.8 V supply voltage in 0.18 µm CMOS technology.

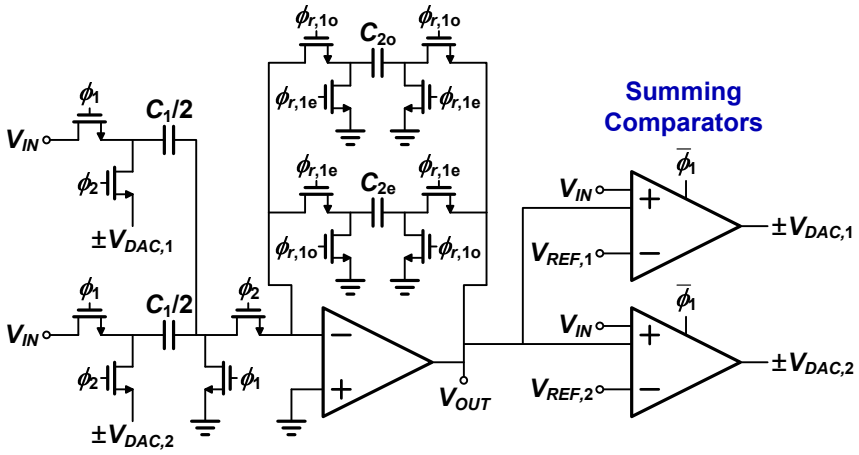
5.1.3 Individual Stage

The architecture of an individual stage for the 8-stage architecture is shown in Fig. 5.2 with a two-phase resetting scheme as illustrated in Fig. 4.10. The sampling capacitor C_1 is split up for the two feedback paths from the 3-level D/A converter. The stage input V_{IN} is fed to the two comparators to implement the input feed-forward architecture. The integrator reset clocks are shown for each of the three OSR configurations of 1, 3 and infinity (no reset).

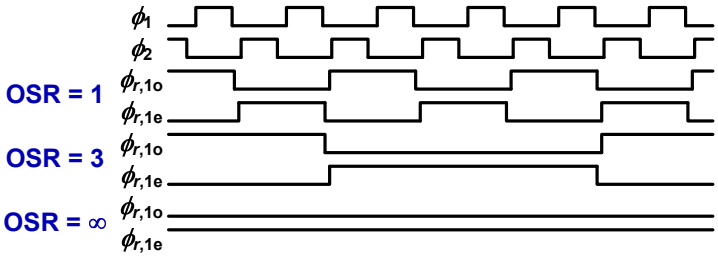
5.1.4 Noise Allocation

With a target resolution of 69 dB for an 8^{th}-order incremental A/D converter with an OSR of 3, the thermal noise floor must be at 72 dB since the incremental converter increases the noise by 3 dB (as discussed in Section 4.3). With this thermal noise floor, the other two architectures should not be thermal noise limited.

The first stage was designed to be twice the size of the second and third stages. The remaining five stages were all eight times smaller than the first stage. Summing the input-referred noise from each stage results in a total noise factor of 0.924 (for a system that relied strictly on the input-referred noise of the first stage with an OSR of 3, this factor would be 0.333). Combining that with the input-referred differential noise from a folded-cascode



(a) Individual Stage



(b) Clocking

Figure 5.2: Individual A/D converter stage and clocking for the three configurations. The two main blocks are the gain/integrator stage and the latched summing comparator.

OTA of $6.3kT/C$ (to be discussed in Section 5.2.5) and a differential peak signal of 0.8 V, the thermal noise floor can be calculated as

$$\begin{aligned} 10\log_{10}\left(\frac{V_s^2}{V_n^2}\right) &= 10\log_{10}\left(\frac{0.8^2/2}{0.924\cdot 6.3kT/C}\right) \\ &= 10\log_{10}\left(1.11x10^{19}C\right) \\ &= 72.0\,\text{dB} \end{aligned} \tag{5.1}$$

for a sampling capacitor C of 1.41 pF at a temperature T of 50 °C. A capacitor of 1.6 pF is used to have some margin on the calculated noise floor. This capacitor dictates sizing for the rest of the circuit.

5.2 Operational Transconductance Amplifier

For the integrator stage shown in Fig. 5.3, which is the basis for the gain or integrator stages in this design, it is important to analyze the DC gain, bandwidth, and slewing current required to meet the target design specifications. The integrator transfer function is

$$\frac{V_{OUT}}{V_{IN}} = \frac{C_1}{C_2}\left(\frac{\dfrac{1}{1+1/A\beta}}{z-\dfrac{1+1/A}{1+1/A\beta}}\right) \tag{5.2}$$

where A is the OTA DC gain and

$$\beta = \frac{C_2}{C_1+C_2+C_{IN}}. \tag{5.3}$$

The sampling capacitor C_1 is 1.6 pF while the integrating capacitor C_2 is 800 fF for an integrator gain coefficient of 2.

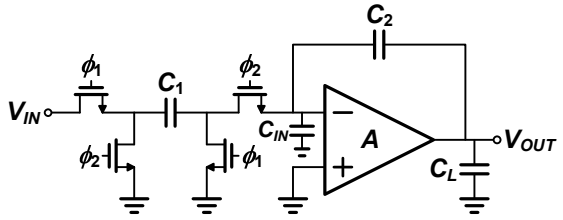


Figure 5.3: Integrator with finite DC gain A, load capacitance C_L, and input capacitance C_{IN}.

5.2.1 DC Gain

With a cascaded architecture, the DC gain needs to be high so that the analog circuitry matches the digital filters. Also, increased OTA gains improve the integrator linearity. With the input feed-forward architecture the OTA output is supposed to contain no signal component, but since only 3-level quantizers are used, the noise is correlated with the input and linearity is still important at the output. A higher resolution quantizer would have whitened the noise introduced by the quantizer at the expense of increased D/A converter levels, making it more difficult to design a linear D/A converter for a given capacitor size.

Simulations were performed with finite DC gain and it was found that for a resolution of 75 dB (a resolution below the thermal noise floor), a finite DC loop gain of 5000 V/V is required in the first stage (see Appendix B). The output spectrum is shown in Fig. 5.4 with a DC gain of 5000 V/V. For subsequent stages, the DC gain requirements are progressively smaller.

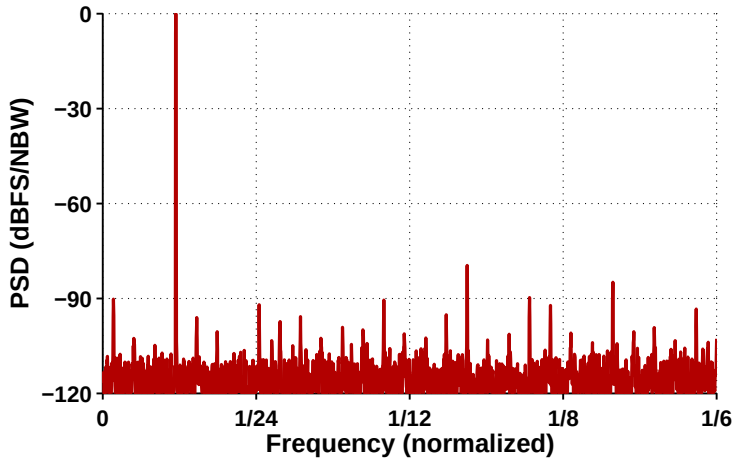


Figure 5.4: Output spectrum for an 8th-order incremental A/D converter with a first stage DC gain of 5000 V/V (NBW $= 1.2 \times 10^{-4}$).

5.2.2 Bandwidth

Since the OTA settling is assumed to be non-linear, it must settle within the accuracy required for the DC gain. For a period T_s, it is assumed that it should settle within the given accuracy in $T_s/4$ seconds to allow some margin for slewing, as well as some time for the non-overlapping clocks.

For a full-scale step input, the output will settle exponentially according to

$$V_{OUT} = 2V_{IN}(1 - e^{-\beta\omega_{unity}t}) \tag{5.4}$$

assuming a single-pole OTA response where the OTA 3 dB-frequency is $\beta\omega_{unity}$ and ω_{unity} is the open-loop OTA unity-gain frequency (without the feedback network β). The error from the ideal output $2V_{IN}$ must be within the accuracy desired after $T_s/4$ seconds. There-

fore,

$$e^{-\beta\omega_{unity}T_s/4} < \frac{1}{2^N} \tag{5.5}$$

for N-bit resolution. Rearranging this equation, the required 3 dB-frequency is

$$\omega_{3dB} = \beta\omega_{unity} > \frac{-4N\ln(2)}{T_s}. \tag{5.6}$$

To keep the settling within the required accuracy at a sampling frequency of 100 MHz, or a period T_s of 10 ns, the OTA must settle to better than 1 part in 5000, or 12.3 bits (assuming a similar accuracy to the finite DC gain from the previous section) for a full-scale output swing in about 2.5 ns. The resulting 3 dB-frequency is 3.47 Grad/s, or 552 MHz.

The previous analysis assumed single-pole settling for the OTA. However, the feed-forward path through capacitor C_2 introduces a zero in the integrator transfer function ω_z that slows down the settling. The settling in Eq. 5.6 must be adjusted to include an extra term, resulting in the inequality

$$\frac{T_s}{4} > \frac{N\ln(2)}{\beta\omega_{unity}} + \frac{\ln(1-\beta\omega_{unity}/\omega_z)}{\beta\omega_{unity}}. \tag{5.7}$$

ω_z is a right-half plane zero so the ratio $\beta\omega_{unity}/\omega_z$ is negative. The zero becomes less significant as β and ω_{unity} decreases. If the load capacitance is reduced to zero, and β is no larger than 1/3, the zero will slow the settling by less than 5%.

Another consideration is the second pole ω_{p2} which influences the settling behaviour. If the system is designed to be critically damped where $\omega_{p2} = 4\beta\omega_{unity}$, then the phase margin will be 76 ° and the system will settle more quickly than the single-pole system. In a critically damped system the output voltage is [72]

$$V_{OUT} = 2V_{IN}(1 - e^{-2\beta\omega_{unity}t} - 2\beta\omega_{unity}te^{-2\beta\omega_{unity}t}). \tag{5.8}$$

For a target resolution of 12.3 bits this requires a $\beta\omega_{unity}$ of 2.10 Grad/s, or 334 MHz, which is about 60% less than with single-pole settling. If the second pole is any smaller, the system will be underdamped, and the settling will get slightly better after which it will get much worse with increased overshoot and reduced phase margin. The target on the second pole is to keep it at around $4\beta\omega_{unity}$ to leave some margin for variations in process,

temperature and voltage.

5.2.3 Slewing

If the OTA undergoes slew-rate limited settling behaviour, the worst-case condition occurs when the OTA output has to supply enough charge through the integrating and load capacitors to fully switch from the highest (or lowest) output voltage to the lowest (or highest) output voltage in the allotted time.

With a differential output swing of $\pm 0.8\,\mathrm{V}$, each side of the OTA could swing by as much as $0.8\,\mathrm{V}$ to charge $C_2 + C_L$ in $T_s/4$ seconds (again it is assumed that one-quarter of the clock period T_s is available for slewing). This results in a required slewing current of

$$\begin{aligned} I_{slew} &= \frac{Q_{max}}{T_s/4} \\ &= \frac{0.8\,\mathrm{V} \cdot (C_2 + C_L)}{T_s/4} \\ &= 320\,\mu\mathrm{A}. \end{aligned} \tag{5.9}$$

A minimum current of $320\,\mu\mathrm{A}$ must be supplied to the OTA branches, depending on the OTA topology. However, due to the high bandwidth requirements of the OTA, the slewing current will not be the limiting factor for the supplied current.

5.2.4 Topology

In $0.18\,\mu\mathrm{m}$ technology the required bandwidth of the OTA is quite high. To attain this speed, a single-stage amplifier is optimal. The gain requirements are also high, requiring a cascoded architecture with gain-boosting. Both a telescopic and a folded-cascode OTA are amenable to gain-boosting and could meet these specifications.

A telescopic OTA is shown in Fig. 5.5. The bandwidth is high because the low-impedance non-dominant pole is at the drain/source terminal of M_1/M_3 where the capacitance of only two transistors contribute to the pole. Increasing L will increase the gain of these transistors, but reduce the bandwidth. Alternatively the gain can be increased by gain-boosting the cascoded transistors M_3, M_4, M_5 and M_6.

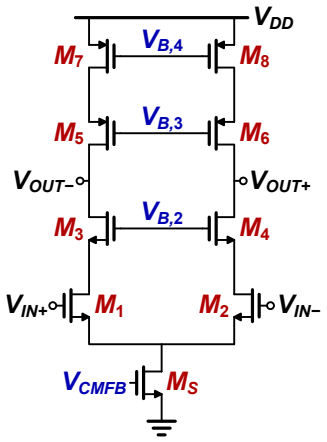


Figure 5.5: Telescopic OTA.

One of the major difficulties with the telescopic OTA is the allowable voltage range on the input and output common-mode levels. The input common-mode voltage range is

$$V_{th} + 2V_{eff} < V_{IN,cm} < V_{OUT,min} - V_{eff} + V_{th}. \tag{5.10}$$

This puts the minimum input common-mode voltage $V_{IN,cm}$ at around 800–900 mV (assuming $V_{th} \approx 500$ mV and $V_{eff} \approx 150$–200 mV). The maximum input common-mode voltage is around 1 V with a 1.8 V supply. With the input common-mode near the mid-rail voltage, the pass transistor at the OTA input needs to be much larger in order to reduce the switch impedance, causing increased charge injection and clock buffer power. Furthermore, since this switch is attached to the sensitive virtual ground terminal of the OTA, it is important to minimize the charge injection at this node.

An alternative OTA topology is the folded-cascode, shown in Fig. 5.6. It was chosen since it does not have the input common-mode limitations of the telescopic OTA. It has a high gain with cascoded transistors, but it is slower than the telescopic OTA since the non-dominant pole at the folding node includes the capacitance of three transistors (M_1, M_3, and M_5) instead of two. Also M_3 is larger than the other transistors since it must sink current from the two branches.

The folded-cascode OTA is also less power efficient since there are 4 current branches rather than 2. If the current branches all use similar currents, then it consumes about twice

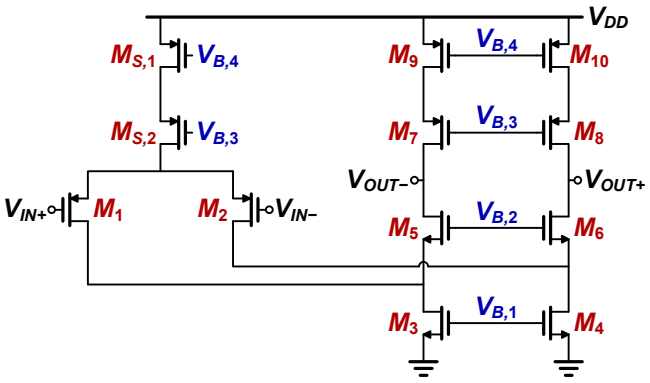


Figure 5.6: Folded-cascode OTA.

as much power as the telescopic OTA. This does not take into account the added power from the clock buffer needed to drive the switches that pass mid-rail voltages for the telescopic OTA.

The output swing is slightly better for the folded-cascode OTA since there are only 4 transistors instead of 5 transistors between the supply rails. Also, an input signal can be passed by a relatively small NMOS transistor since the input common-mode can be lower (as low as ground) without causing any transistors to enter the triode region.

5.2.5 Thermal Noise

The thermal noise of a folded-cascode OTA can be found by input-referring all the noise sources. Referring to Fig. 5.7, noise sources are considered at all the current-source transistors but not the cascode transistors because the cascode transistors contribute very little to the total noise [63]. Also, the noise current $I_{n,S}$ contributes equally to both sides of the differential amplifier and does not contribute to the differential noise.

The noise current *power spectral density* (PSD) for each transistor is $\overline{I_n^2} = 4kT\gamma g_m$ where γ is a coefficient that depends on the transistor length and is 2/3 for long-channel devices [63]. Output-referring each uncorrelated noise source and then input-referring it through the OTA gain, the resulting total input-referred noise voltage PSD is

$$\overline{V_n^2} = 2\frac{\overline{I_{n,1}^2} + \overline{I_{n,3}^2} + \overline{I_{n,9}^2}}{g_{m,1}^2}$$

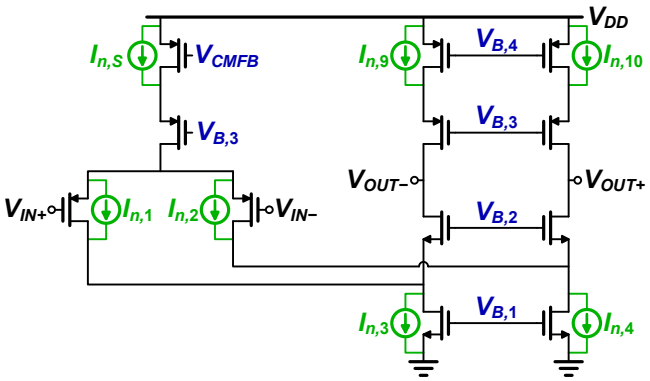


Figure 5.7: Noise sources in a folded-cascode OTA. The cascoded transistors do not contribute significantly to the total noise.

$$= 2\frac{4kT\gamma g_{m,1} + 4kT\gamma g_{m,3} + 4kT\gamma g_{m,9}}{g_{m,1}^2}$$
$$= \frac{8kT\gamma}{g_{m,1}}\left(1 + \frac{g_{m,3}}{g_{m,1}} + \frac{g_{m,9}}{g_{m,1}}\right). \tag{5.11}$$

If the bias currents through M_1 and M_9 are the same so that M_3 has twice the current as M_1 and M_9, the noise voltage PSD is

$$\overline{V_n^2} = \frac{8kT\gamma}{g_{m,1}}\left(1 + 2\frac{V_{eff,1}}{V_{eff,3}} + \frac{V_{eff,1}}{V_{eff,9}}\right)$$
$$= \frac{8kT\gamma}{g_{m,1}} n_f \tag{5.12}$$

where the parameter n_f has been used to indicate the increased noise voltage relative to an OTA where the input differential pair dominates the noise voltage. From this equation it is clear that the input-referred thermal noise from the OTA is a function of the relative effective voltages of the various transistors. In older technologies V_{eff} could be made much larger and n_f could be considered unity, but in more recent technologies with limited headroom the V_{eff} of different transistors will not vary by much more than a factor of 2, increasing the impact of n_f.

For a power-efficient architecture where the transconductance dominates the bandwidth (rather than the switch resistance), the total differential input-referred thermal noise power

of the switched-capacitor integrator shown in Fig. 5.3 is [73, 74]

$$\overline{V_{int}^2} = \frac{kT}{C_1}(4n_f/3+2). \tag{5.13}$$

If all the effective voltages are the same, the resulting noise power is $7.33kT/C_1$. If $V_{eff,3} = V_{eff,9} \approx 2V_{eff,1}$, then the noise power is $5.33kT/C_1$. With the chosen effective voltages ($V_{eff,1} \approx 150\,\text{mV}$, $V_{eff,3} = V_{eff,9} \approx 200\,\text{mV}$), the noise power for this design is about $6.3kT/C_1$. Note that the effective voltages are chosen based on a number of factors including noise, output swing, speed, input capacitance and feedback factor β. Some of these factors are discussed in the next section.

5.2.6 Choice of Effective Voltage

When designing a power-efficient high-speed amplifier, it is important to choose effective voltages that optimize the speed and the transistor efficiency. A single transistor in 0.18 µm can be analyzed to find the optimal V_{eff} for speed and power. With a length of 0.24 µm, the bias current of a transistor in saturation is swept and its efficiency g_m/I_d is measured as well as its unity-gain frequency f_t. The product of these parameters gives a figure of merit that helps determine a starting point for the optimal speed and efficiency V_{eff} bias of a differential pair.

Fig. 5.8 shows the the speed-efficiency figure of merit plotted against the effective voltage for a 0.24 um NMOS transistor. The optimal effective voltage is 155 mV. Assuming that there will likely be some variations in the effective voltage from the designed value, it is better to bias the transistor slightly higher than 155 mV. A similar plot can be made for a PMOS transistor and the optimal effective voltage is 205 mV and is shown in Fig. 5.9. In order for a unit sized NMOS and PMOS transistor to have similar relative efficiencies (for the same I_d and L), the PMOS transistor should be 3 times larger (in this design a factor of 4 was typically used).

Other trade-offs exist when choosing the effective voltages. The non-dominant pole location can significantly affect the settling behaviour, and adjusting the size of transistors M_3-M_6 can move the non-dominant pole accordingly. The effective voltages found from Fig. 5.8 and Fig. 5.9 are good starting points.

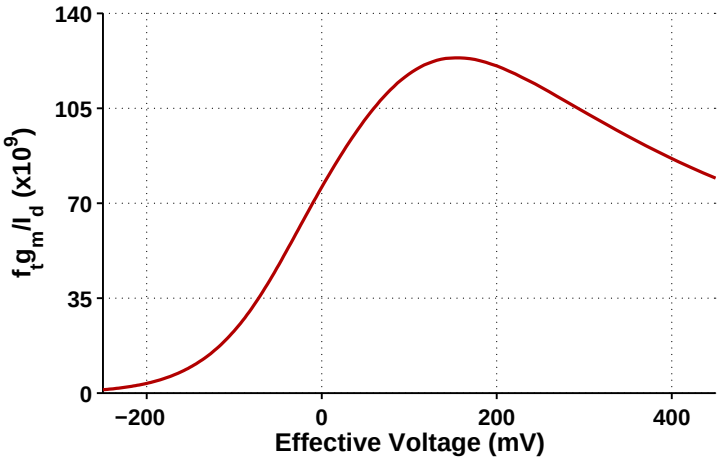


Figure 5.8: Speed-Efficiency Product vs. Effective Voltage for an NMOS device. The optimal effective voltage is 155 mV.

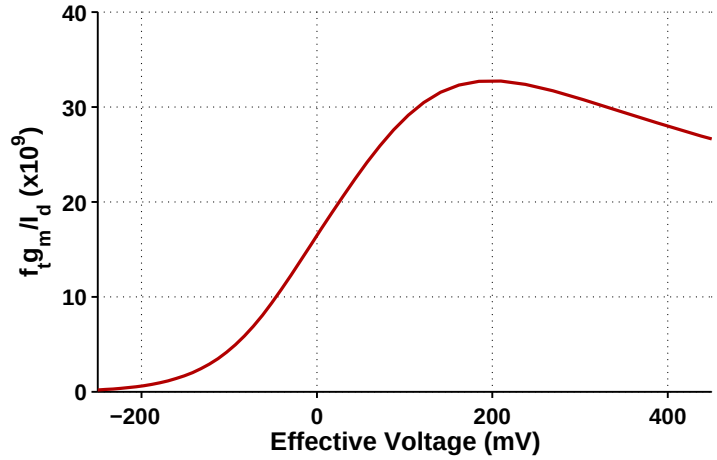


Figure 5.9: Speed-Efficiency Product vs. Effective Voltage for a PMOS device. The optimal effective voltage is 205 mV.

5.2.7 Design

The initial sizes for a unit-sized amplifier are shown in Fig. 5.10. Transistor sizes are based on the desired V_{eff} at a bias current of 50 µA for each branch. All the transistors have a length of 0.24 µm except for the input differential pair whose length is 0.18 µm to reduce the OTA input capacitance and increase the transconductance of the input pair. The

input transistor widths are chosen based on a trade-off between input capacitance (which reduces β and hence the 3 dB-frequency) and transconductance (which increases the 3 dB-frequency).

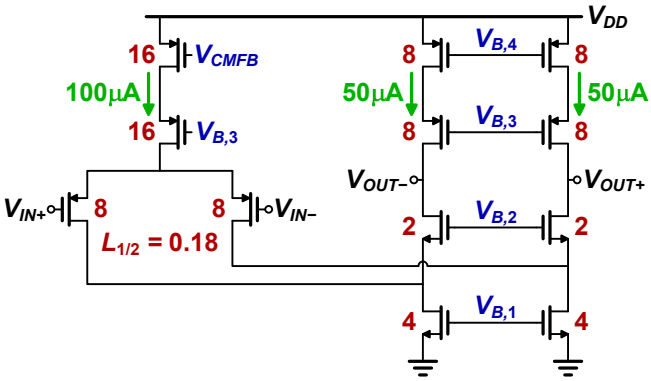


Figure 5.10: Transistors sizes for the folded-cascode OTA. All sizes are in microns, and all transistor lengths are 0.24 µm unless otherwise noted.

The OTA input and output branches have equal currents. It is advantageous to put more current in the input branches to increase the g_m, and less current in the output branches to increase the output impedance r_o. However, if the OTA slews, the input branch transistors will go into the triode region which will slow down the OTA, reduce the gain, and cause distortion. Therefore the output branch currents must be greater than or equal to the input branch currents, the optimal choice being equal.

The unit-sized OTA of Fig. 5.10 needs to be scaled (i.e., increasing the number of fingers for all the transistors equally) until it can properly drive the integrator capacitors C_1 and C_2 which are 1.6 pF and 800 fF, respectively. An optimal bandwidth can be found for high-speed operation. Initially the bandwidth increases with the number of fingers $N_{fingers}$ because the bandwidth is

$$\omega_{3dB} = \beta\,\omega_{unity} = \beta\, g_{m,1}/C_{eff} \tag{5.14}$$

where

$$C_{eff} = \frac{C_2(C_1 + C_{IN})}{C_2 + C_1 + C_{IN}} + C_L \tag{5.15}$$

and

$$\beta = \frac{C_2}{C_2 + C_1 + C_{IN}} \tag{5.16}$$

and the transconductance $g_{m,1}$ increases linearly with $N_{fingers}$ while β and C_{eff} are rela-

tively constant (as long as C_{IN} is much smaller than C_1). Since $C_{IN} \propto N_{fingers}$, eventually as $N_{fingers}$ increases, C_{IN} will be much larger than C_1 (and C_2). At this point β will decrease linearly with $N_{fingers}$, negating any linear increases of $g_{m,1}$ with $N_{fingers}$, but C_{eff} will increase because the first term in Eq. 5.15 will be constant while C_L will begin to increase due to self-loading of the output transistors. The net effect is a decrease in bandwidth. Somewhere in between there will be a value of $N_{fingers}$ where a peak amplifier bandwidth is obtained.

Fig. 5.11 plots the 3 dB-frequency for increasing $N_{fingers}$. The peak 3 dB-frequency of 693 MHz occurs at 69 fingers. $N_{fingers} = 64$ is chosen as a reasonable value with enough margin for the 3 dB-frequency (given that gain-boosting has not yet been added). With 64 fingers the phase margin is 81.4 ° and the DC loop gain is 33.6 dB. Obviously the DC gain is far too low, but gain-boosting can increase the gain to the desired value. The frequency and phase response of the amplifier are shown in Fig. 5.12.

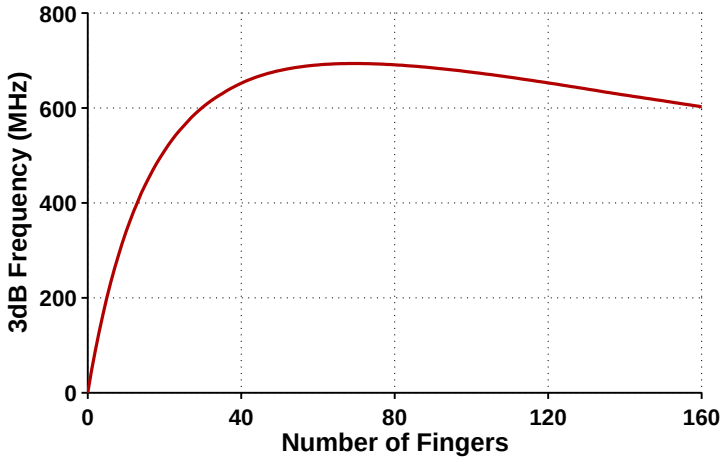


Figure 5.11: 3 dB-Frequency vs. Number of Fingers. The highest bandwidth occurs with 69 fingers.

A lot of power is wasted when a high 3 dB-frequency is required, as evidenced by the plot of Fig. 5.11. Towards the peak of the curve the bandwidth no longer increases linearly with the number of fingers, resulting in a less power-efficient architecture than when lower bandwidth amplifiers are designed in the same technology. This is a shortcoming of trying to increase bandwidth in a given technology; figure of merits will tend to be much worse due to the inefficient trade-off between power and bandwidth.

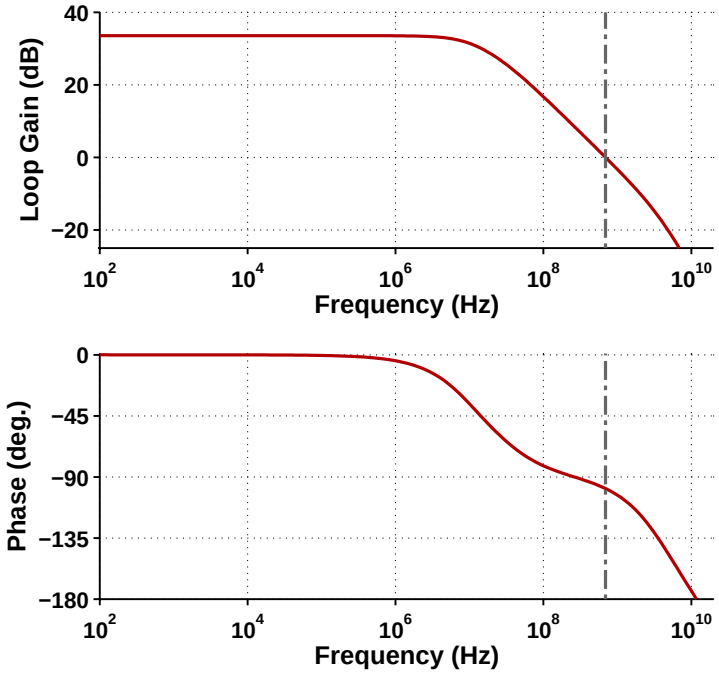


Figure 5.12: Bode plot of the folded-cascode OTA with 64 fingers.

5.2.8 Gain-Boosting

Gain-boosting can further increase the DC gain of an OTA while theoretically decoupling it from the OTA bandwidth [75]. Both the PMOS and NMOS cascoded transistors in the output branch of the folded-cascode OTA are gain-boosted as shown in Fig. 5.13.

Stability and Settling

It is important to design the gain-boosted amplifiers properly so that they do not significantly affect the OTA settling behaviour. The gain-boosting path adds a pole-zero doublet in the OTA transfer function. This can be seen by analyzing Fig. 5.14 which is a portion of the output branch in the main amplifier. The output impedance without gain-boosting is

$$Z_{OUT,1} = \frac{R_o}{1 + sR_oC_L} \tag{5.17}$$

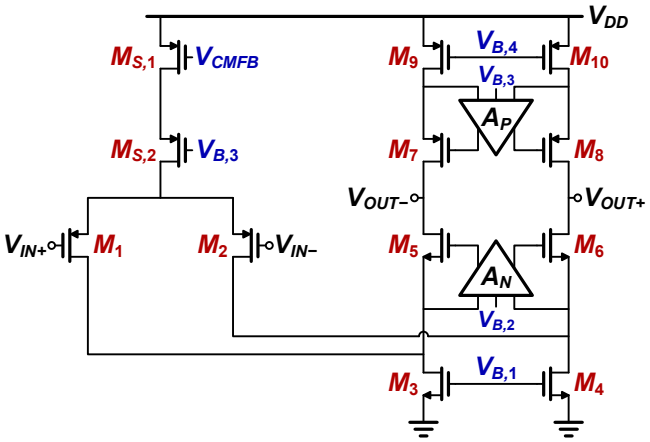


Figure 5.13: Gain-boosted folded-cascode OTA.

where

$$\begin{aligned} R_o &= r_{o,3} + r_{o,5} + g_{m,5} r_{o,3} r_{o,5} \\ &\approx g_{m,5} r_{o,3} r_{o,5} \end{aligned} \tag{5.18}$$

Ignoring the non-dominant pole at the drain of M_3, the output impedance has a first-order response.

If the gain-boosted output impedance is analyzed, and it is assumed that the amplifier A has a DC gain of A_o with a 3 dB-frequency $1/RC$, the output impedance is

$$\begin{aligned} Z_{OUT,2} &= R_o(A+1) \left\| \frac{1}{sC_L} \right. \\ &= R_o \left(\frac{A_o}{1+sRC} + 1 \right) \left\| \frac{1}{sC_L} \right. \\ &= R_o(A_o+1) \frac{(1+s/\omega_z)}{(1+s/\omega_{p,1})(1+s/\omega_{p,2})} \end{aligned} \tag{5.19}$$

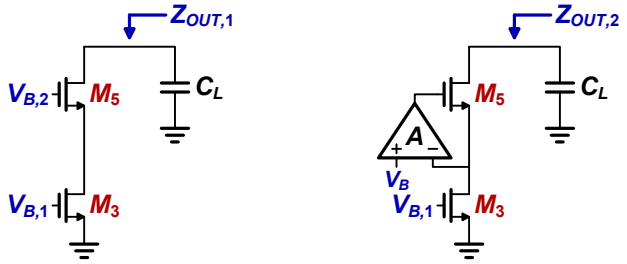
where

$$\omega_z = \frac{1+A_o}{RC} \tag{5.20}$$

$$\omega_{p,1} \approx \frac{1}{R_o C_L (1+A_o)} \Big/ \left(1 + \frac{RC}{R_o C_L A_o} \right) \tag{5.21}$$

$$\omega_{p,2} \approx \omega_z \Big/ \left(1 - \frac{RC}{R_o C_L A_o}\right) \tag{5.22}$$

assuming that $A_o \gg 1$. The 3 dB-frequency of the additional amplifier $1/RC$ has to be larger than the 3 dB-frequency of the main amplifier $1/R_oC_L$ to maintain a first-order roll-off for the entire circuit [75], meaning that the denominator in Eq. 5.21 is going to be close to 1. The zero and second-pole frequency are roughly equal to the unity-gain frequency of the additional amplifier.



(a) No Gain-Boosting (b) Gain-Boosting

Figure 5.14: Output impedance without and with gain-boosting.

More importantly, however, is the pole-zero doublet that occurs. The zero frequency ω_z is similar to the second-pole frequency $\omega_{p,2}$, and they only differ because of the extra term in the denominator of Eq. 5.22 which is close to unity. While the difference is small, it is not zero, so the zero and the second-pole do not perfectly cancel, resulting in a pole-zero doublet. This can influence the settling behaviour of the closed-loop amplifier because in the presence of the additional doublet, the resulting settling behaviour of a single-pole system becomes [76]

$$V_{OUT} \approx V_{IN}(1 - e^{-\beta\omega_{unity}t} + \frac{\omega_z - \omega_{p,2}}{\beta\omega_{unity}} e^{-\omega_z t}). \tag{5.23}$$

where $\beta\omega_{unity}$ is the closed-loop 3 dB-frequency of the single-pole system. An extra settling component exists with the additional $e^{-\omega_z t}$ term. In order for it to be faster and less significant than the dominant settling term $e^{-\beta\omega_{unity}t}$, it must be designed so that $\omega_z > \beta\omega_{unity}$. The magnitude of the extra settling component is

$$\left|\frac{\omega_z - \omega_{p,2}}{\beta\omega_{unity}}\right| = \left|\frac{1+A_o}{\beta\omega_{unity}RC}\left(1 - 1\Big/\left(1 - \frac{RC}{R_oC_LA_o}\right)\right)\right|$$

$$\approx \frac{1}{\beta \omega_{unity} R_o C_L}. \tag{5.24}$$

This is approximately equal to the reciprocal of the OTA loop gain without gain-boosting (since $\omega_{unity} \approx g_m R_o \omega_{3dB} = g_m/C_L$), which is significant relative to the required settling accuracy that is A_o times larger.

There is one remaining constraint on the location of the zero frequency ω_z (which is also the unity-gain frequency of the additional amplifier) relative to the second pole of the additional amplifier ω_2. Note that this pole has not yet been considered and should not to be confused with the second pole of the main amplifier $\omega_{p,2}$. For a stable amplifier stage, the second pole of this additional amplifier ω_2 should be larger than the unity-gain freqeuncy of the amplifier loop ω_2 [75] (when they are equal, the phase margin will be 45°). For a phase margin of 76° it should be 4 times larger, but the phase margin does not need to be quite as high as in the main amplifier since these voltage levels should be fairly stable. ω_z, or the unity-gain frequency of the additional amplifier, is therefore constrained according to the inequality

$$\beta \omega_{unity} < \omega_z < \omega_2. \tag{5.25}$$

Sizing

With these constraints in mind, a differential gain-boosting amplifier is used since it is more likely to have a unity-gain frequency larger than $\beta \omega_{unity}$ of the main amplifier. It is difficult to design a single-ended gain-booster that meets these requirements since the main amplifier was already optimized to have a fairly high bandwidth. An added benefit with a differential gain-booster is the increased *common-mode rejection ratio* (CMRR). The differential gain of the gain-boosted main amplifier is increased by the gain of the gain-boosters while the common-mode gain is only increased by the common-mode gain of the gain-boosters.

The two gain-boosters are similar to the main amplifier; they are both folded-cascode OTAs. The gain-booster for the PMOS cascodes has NMOS input transistors due to the high common-mode input voltage and is shown in Fig. 5.15. The gain-booster for the NMOS cascodes has PMOS inputs and is similar to the main amplifier shown in Fig. 5.6.

The transistor sizes for the gain-boosters are summarized in Table 5.1 and Table 5.2. The PMOS-input gain-booster is smaller because it controls the gates of cascoded NMOS

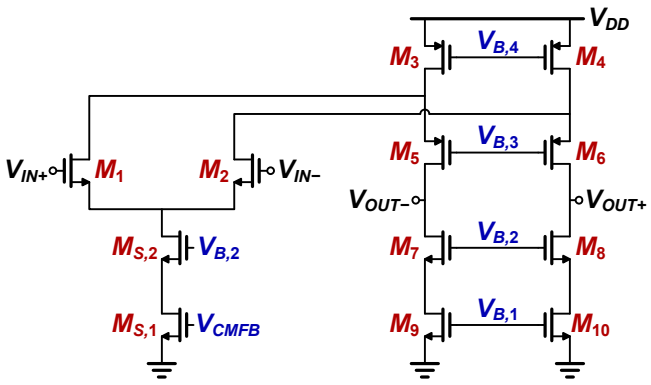


Figure 5.15: Folded-cascode OTA with NMOS input for gain-boosting amplifier A_P.

transistors rather than cascoded PMOS transistors with the same current density, resulting in a smaller gate capacitance to drive.

Transistor	Type	Fingers	Width	Length	Current
$M_{S,1}$, $M_{S,2}$	NMOS	48	2 µm	0.24 µm	2.4 mA
M_1, M_2	NMOS	24	2 µm	0.18 µm	1.2 mA
M_3, M_4	PMOS	48	8 µm	0.24 µm	2.4 mA
M_5, M_6	PMOS	24	8 µm	0.24 µm	1.2 mA
M_7-M_{10}	NMOS	24	2 µm	0.24 µm	1.2 mA

Table 5.1: Sizing for gain-booster A_P (Fig. 5.15).

Transistor	Type	Fingers	Width	Length	Current
$M_{S,1}$, $M_{S,2}$	PMOS	16	8 µm	0.24 µm	0.8 mA
M_1, M_2	PMOS	8	8 µm	0.18 µm	0.4 mA
M_3, M_4	NMOS	16	2 µm	0.24 µm	0.8 mA
M_5, M_6	NMOS	8	2 µm	0.24 µm	0.4 mA
M_7-M_{10}	PMOS	8	8 µm	0.24 µm	0.4 mA

Table 5.2: Sizing for gain-booster A_N (Fig. 5.6).

Common-Mode Feedback

A *common-mode feedback* (CMFB) circuit is necessary since the gain-boosters are differential rather than single-ended. A continuous-time circuit can be used because a large swing is not required at the output of the gain-boosting amplifier. For the gain-booster A_P, the chosen CMFB circuit [45] is shown in Fig. 5.16. The output voltages are compared against the desired output common-mode voltage $V_{B,3}$, and the diode connected transistor M_6 adjusts the tail-current source of the gain-booster if the common-mode output voltage is too high or low. The current source transistors $M_{S,1}$ and $M_{S,2}$ are not cascoded since the common-mode output voltage is fairly high and with cascoding there would be a risk of pushing the current sources into the triode region.

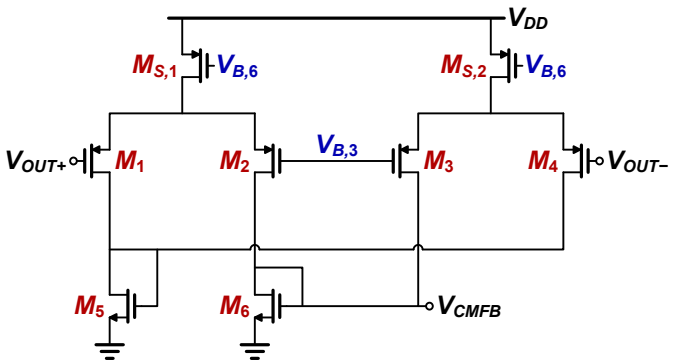


Figure 5.16: CMFB circuit for gain-booster A_P (Fig. 5.15).

A similar circuit with NMOS input differential pairs is used for the other gain-booster A_N. This circuit is shown in Fig. 5.17. Again the current source transistors $M_{S,1}$ and $M_{S,2}$ are not cascoded since the common-mode output voltage is too low.

The transistor sizes for the continuous-time CMFB circuits are summarized in Table 5.3 and Table 5.4. They are both similarly sized, with similar current densities in the corresponding transistors.

The CMFB loop must also be analyzed to ensure stability. With the CMFB circuit controlling the entire transistor $M_{S,1}$ (of Fig. 5.15), the phase margin is too low. The CMFB loop for gain-booster A_P has a phase margin above 60° when the 16 fingers of the current source transistor $M_{S,1}$ is split so that only 6 fingers are controlled by the CMFB circuit. Similarly, the CMFB loop for gain-booster A_N has a phase margin above 60° when only

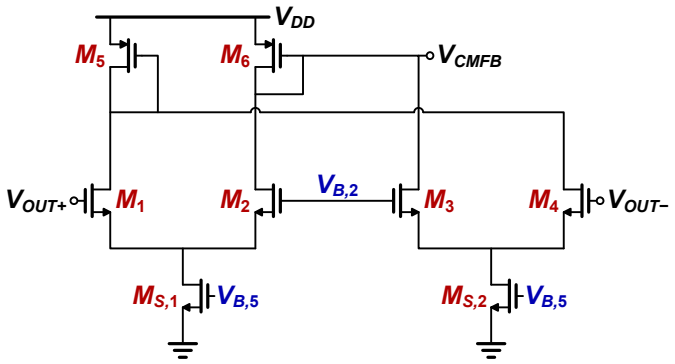


Figure 5.17: CMFB circuit for gain-booster A_N (Fig. 5.6).

Transistor	Type	Fingers	Width	Length	Current
$M_{S,1}$, $M_{S,2}$	PMOS	8	8 µm	1 µm	100 µA
M_1-M_4	PMOS	4	8 µm	0.24 µm	50 µA
M_5, M_6	NMOS	2	2 µm	0.24 µm	100 µA

Table 5.3: Sizing for CMFB circuit of Fig. 5.16.

Transistor	Type	Fingers	Width	Length	Current
$M_{S,1}$, $M_{S,2}$	NMOS	4	2 µm	1 µm	50 µA
M_1-M_4	NMOS	2	2 µm	0.24 µm	25 µA
M_5, M_6	PMOS	1	8 µm	0.24 µm	50 µA

Table 5.4: Sizing for CMFB circuit of Fig. 5.17.

16 of the 48 current source transistor fingers ($M_{S,1}$ of Fig. 5.6) are controlled by the CMFB circuit.

Simulations

The gain-booster A_P is loaded with a 200 fF capacitor as well as the gate capacitance from the main amplifier's PMOS cascode transistor. The DC gain is 47.4 dB and the unity-gain frequency is 879 MHz, which is larger than $\beta\omega_{unity}$ of the main amplifier and smaller

than the second-pole frequency, as desired. The loop bode plot with the PMOS cascoded transistor acting as a source follower is shown in Fig. 5.18. The source follower introduces a low gain of 0.72 V/V due to the body effect (the bulk is not connected the source). The loop phase margin is 70.4 °.

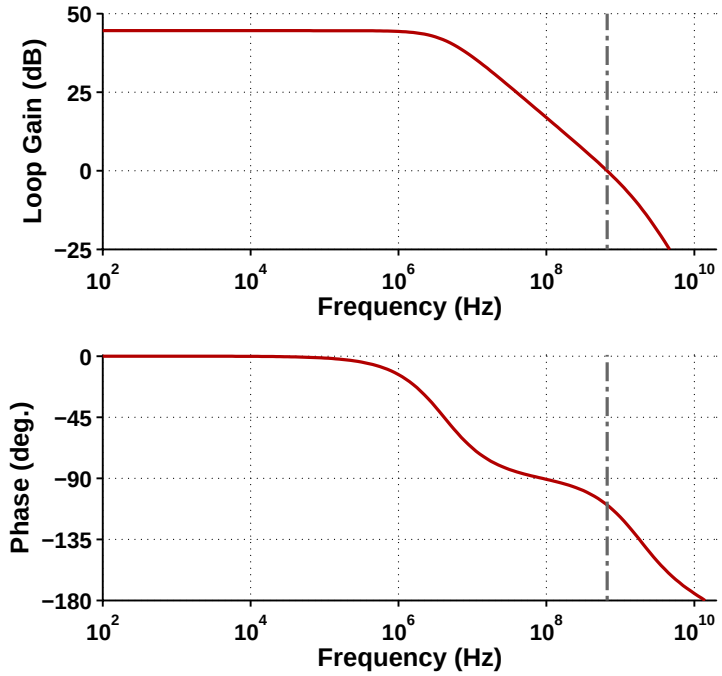


Figure 5.18: Bode plot of gain-booster A_P (Fig. 5.15).

The other gain-booster A_N is loaded with a 100 fF capacitor as well as the gate capacitance from the main amplifier's NMOS cascode transistor. This amplifier is faster and consumes less power since it drives NMOS transistors. The DC gain is 47.6 dB and the unity-gain frequency is 1099 MHz, which is also larger than $\beta\omega_{unity}$ of the main amplifier and smaller than the second-pole frequency. The loop bode plot including the NMOS source follower is shown in Fig. 5.19. The source follower adds a gain of 0.75 V/V and the bulk is also not connected to the source. The phase margin of the loop is 77.5 °.

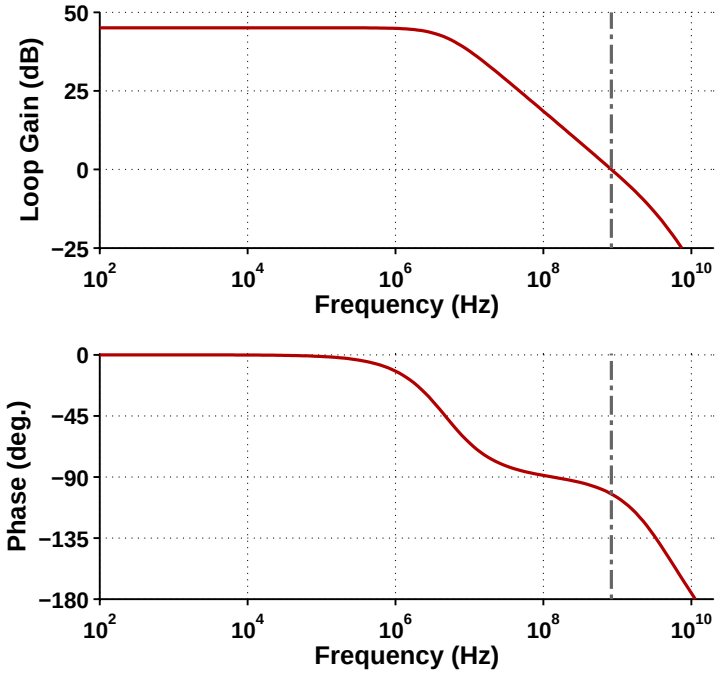


Figure 5.19: Bode plot of gain-booster A_N (Fig. 5.6).

5.2.9 Main OTA Common-Mode Feedback

For the main OTA of a switched-capacitor A/D converter, a switched-capacitor CMFB circuit is used that does not limit the output swing like some continuous-time CMFB circuits. The chosen CMFB circuit is shown in Fig. 5.20 [77]. The node V_{CMFB} controls the bias voltage of transistor $M_{S,1}$ in Fig. 5.10. The switched-capacitor circuit acts as a low-pass filter on the DC bias voltages $V_{OUT,CM}$ and $V_{B,4}$, gradually charging C_2 up to the desired voltage which is the difference between $V_{OUT,CM}$ and $V_{B,4}$. On ϕ_1, V_{CMFB} will be the average of the two output voltages V_{OUT+} and V_{OUT-}, offset by the voltage difference of $V_{OUT,CM}$ and $V_{B,4}$ to properly control the tail current source $M_{S,1}$.

Sizing

C_1 is sized smaller than C_2 so that glitches in the output common-mode voltage are minimized. With a large C_1, the charge sharing from C_1 to C_2 would have a more dramatic

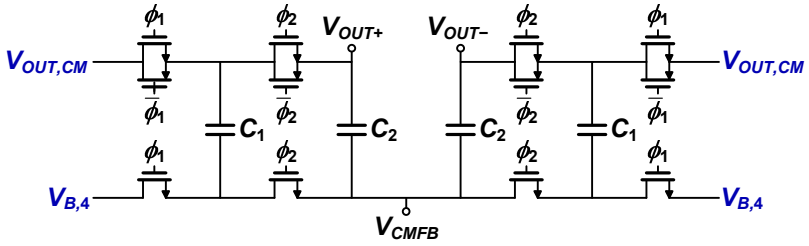


Figure 5.20: Switched-capacitor common-mode feedback.

impact on the charge added to C_2 during ϕ_2, resulting in potential glitches at the tail current source voltage V_{CMFB}.

The transistors in Fig. 5.20 are minimum size so that charge injection errors do not impact the voltages on C_1 and C_2 significantly. Also for this reason, C_1 and C_2 are not too small, but they are kept small enough so that C_2 does not heavily load the main amplifier. For the first-stage amplifier, C_1 is 100 fF while C_2 is 200 fF.

Stability

The CMFB stability was also analyzed. The loop is shown in Fig. 5.21 where the input is at the gate of the tail current source transistor $M_{S,1}$ while the output is at the node between the CMFB capacitors and the parasitic capacitance C_P from the gate of the current source $M_{S,1}$.

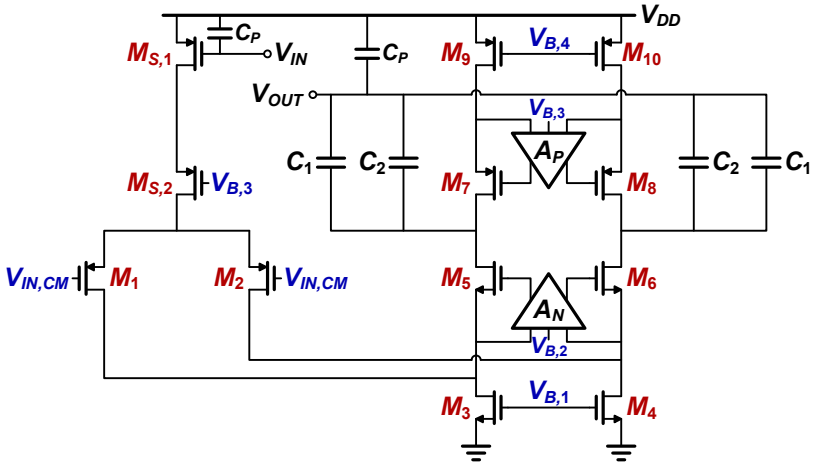


Figure 5.21: Stability analysis of the CMFB loop.

The parasitic capacitance C_P is significant when analyzing the stability of the CMFB circuit. If the phase margin is too low, the gain can be reduced to stabilize the CMFB circuit. This can typically be accomplished by allowing the CMFB circuit to control only a fraction of the transistor $M_{S,1}$, thereby reducing $g_{m,S1}$ in the CMFB loop gain keeping all other parameters equal, resulting in an overall loss of gain. However, if C_P is much larger than $C_1 + C_2$, then

$$\begin{aligned} V_{OUT} &\propto g_{m,S1} \frac{C_1 + C_2}{C_1 + C_2 + C_P} \\ &\approx g_{m,S1} \frac{C_1 + C_2}{C_P}. \end{aligned} \tag{5.26}$$

Since both C_P and $g_{m,S1}$ scale with each other, reducing the size of $M_{S,1}$ in the CMFB loop has no impact (to a first-order approximation) on the CMFB gain as long as C_P is large, as was the case in this design. If the gain needs to be reduced, C_2 and C_1 need to be decreased. The chosen values of 200 fF and 100 fF were sufficient to give the CMFB loop a phase margin of 77.5 ° with a DC gain of 32.7 dB. The bode plot of the CMFB loop is shown in Fig. 5.22.

5.2.10 Gain-Boosted OTA

With the gain-boosters discussed in the previous section, the main amplifier was simulated differentially to ensure that the overall DC gain, phase margin, and bandwidth were as expected. The bode plot of the gain-boosted folded-cascode amplifier loop is shown in Fig. 5.23. The DC gain is 79.1 dB, the phase margin is 74.7 °, and the unity-gain frequency is 633 MHz. The common-mode gain with feedback is also stable since the gain is less than unity.

The bode plot of Fig. 5.23 assumes the OTA is being operated during the integrating/gain phase (ϕ_2 of Fig. 5.3). However, the sampling phase ϕ_1 must also be stable. The stages are sized such that the second stage is half the size of the first stage, so the second stage sampling capacitor is the same size as the first stage feedback capacitor, or $C_L = C_2$ in Fig. 5.3. The ϕ_1 phase is less stable than the ϕ_2 phase since the feedback factor β is increased. On phase ϕ_1 the DC gain is 83.5 dB, the phase margin is 67.5 °, and the unity-gain frequency is 897 MHz.

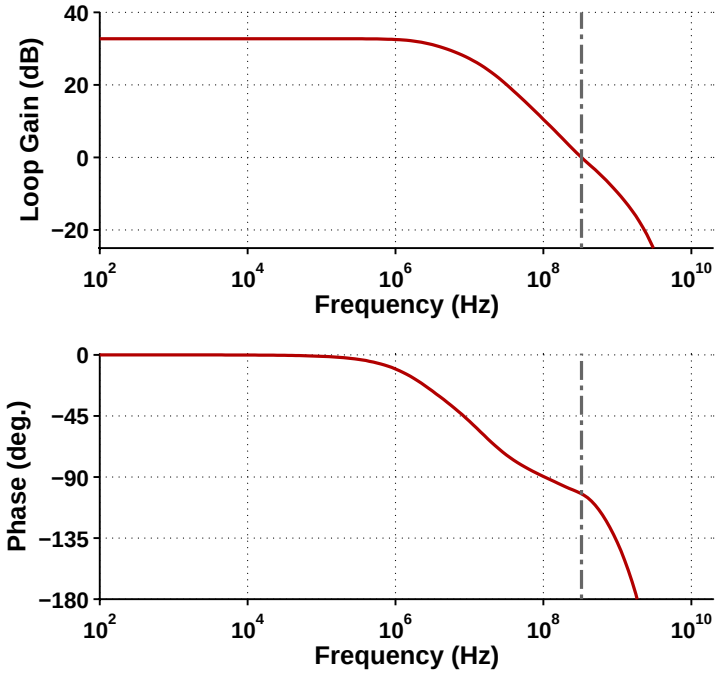


Figure 5.22: Bode plot of the switched-capacitor CMFB loop.

Bode plots are not sufficient for determining how well a circuit will operate. The transient behaviour of the circuit must be simulated to ensure proper settling behaviour within the allotted time period. Fig. 5.24 shows the OTA settling with a full-scale output of ± 800 mV. It settles to 1 part in 5000 within 2.486 ns, and the zero accounts for 0.119 ns of the settling. These values are within the expected range for an OTA with a 633 MHz bandwidth where extra poles, the zero, and the pole-zero doublet will cause the OTA settling to be more complicated than a simple second-order response.

5.2.11 Stage Scaling

Table 5.5 summarizes the relative scaling used for each stage. The main OTA and gain-boosters are all scaled relative to their respective unit-sized amplifiers (as presented in the previous sections).

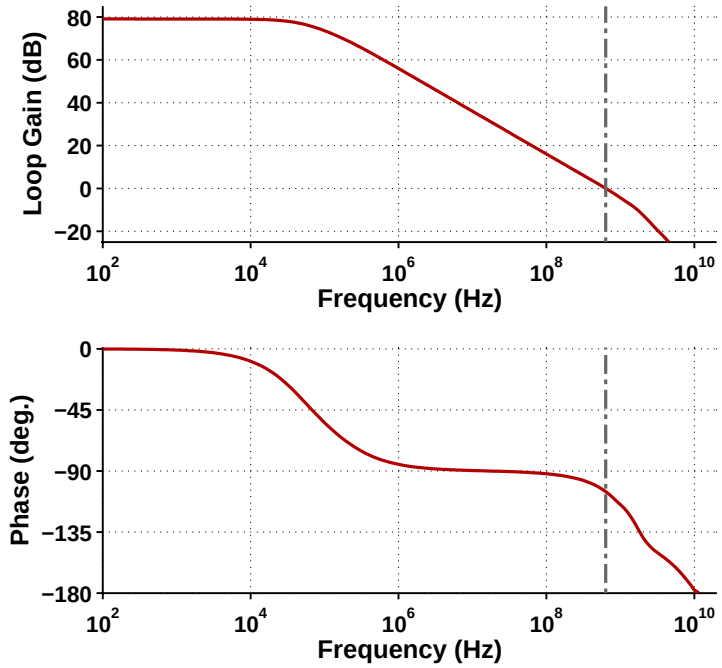


Figure 5.23: Bode plot of the gain-boosted folded-cascode OTA.

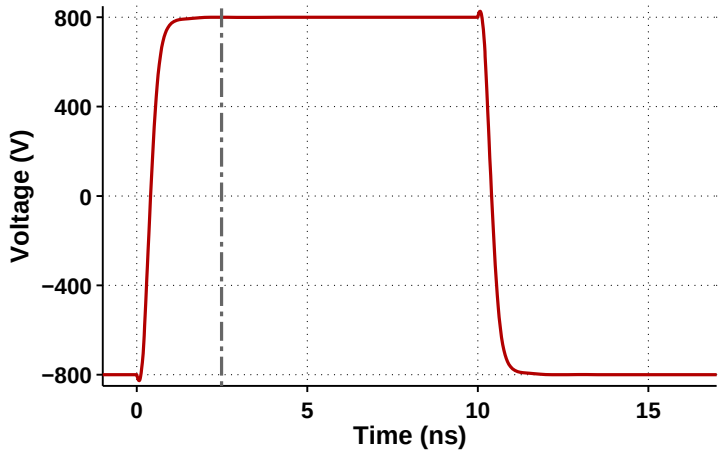


Figure 5.24: Settling behaviour of the gain-boosted folded-cascode OTA with a full-scale output votlage between $\pm 800\,\mathrm{mV}$.

Stage	Sampling Capacitor	Main OTA (relative size)	Gain-Booster A_P (relative size)	Gain-Booster A_N (relative size)
1	1.6 pF	8	6	4
2	800 fF	4	3	2
3	800 fF	4	3	2
4	200 fF	1	1	1
5	200 fF	1	1	1
6	200 fF	1	1	1
7	200 fF	1	1	1
8	200 fF	1	1	1

Table 5.5: Relative stage scaling for the main OTA and gain-boosters.

5.3 Other Circuits

5.3.1 Summing Analog-to-Digital Converter

The 3-level comparison is made with two identical summing comparators as shown in Fig. 5.2, and a single summing comparator is shown in Fig. 5.25. The summing comparator doubles the value of the feed-forward term $V_{IN,2}$ from the previous stage and adds it to the current stage's OTA output $V_{IN,1}$. The comparison is then made by a fast, resistor-loaded preamplifier followed by a latch. Speed is important because the comparator latches on $\overline{\phi_1}$ it is expected to have valid output through the D/A converter within the non-overlap time. If the output is not valid within this time, then the comparator begins to use some of the OTA settling time to resolve its comparison, necessitating a faster OTA.

Each summing comparator has a V_{REF} voltage according to the desired comparison. A passive summer is used at the comparator input since no extra active components are required. The voltage at the input to the comparator is

$$V_P = \frac{2V_{IN,2} + V_{IN,1} - 3V_{REF}}{3 + C_P/C}. \tag{5.27}$$

The summing comparator introduces an attenuation of $3 + C_P/C$. While this attenuates the signal at the comparator input, it is also a necessary attenuation since both $V_{IN,1}$ and $V_{IN,2}$

have voltages of $\pm 800\,\text{mV}$ (differentially). If the summation $2V_{IN,2} + V_{IN,1}$ of these two terms remains unattenuated, the input to the preamplifier would be too large for a 1.8 V circuit, potentially turning off one side of the preamplifier input pair. An attenuation of $3 + C_P/C$ keeps the input to the preamplifier below $\pm 800\,\text{mV}$. A gain error is introduced due to the parasitic capacitance C_P, but it only scales the voltage at V_P, not the relative voltages. Since the reference voltage V_{REF} is embedded in the voltage at V_P, the comparison against zero remains unchanged.

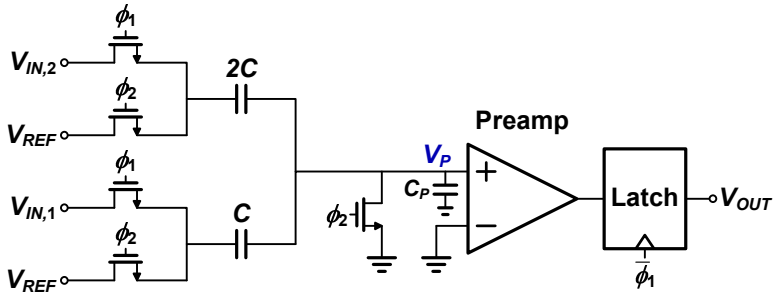


Figure 5.25: Comparator with passive summer. The feed-forward input from the previous stage $V_{IN,2}$ is added to the OTA output from the current stage $V_{IN,1}$.

Preamplifier

The resistor-loaded preamplifier is shown in Fig. 5.26. The preamplifier lowers the matching requirements on the subsequent latch stage, and it also helps decouple the noisy latch from the input signals and reference voltages.

The resistor is sized for a preamplifier gain of 5. The input differential pair is sized according to threshold mismatch variations $\sigma_{VT} = A_{VT}/\sqrt{WL}$. Based on simulations of a non-ideal incremental A/D converter, the first-stage quantizer can tolerate a matching error of $\sigma = 10\%$ where the SNDR will be greater than 75 dB with 99% yield, resulting in an input pair area if at least $0.1\,\mu\text{m}^2$. The output common-mode of the preamplifier is 1.2 V, the resistors are $6\,\text{k}\Omega$, the current is $200\,\mu\text{A}$, and the input transistors are $4\,\mu\text{m}$ by $0.18\,\mu\text{m}$.

Latch

The latch input pair is smaller than the preamplifier and is shown in Fig. 5.27. The gain of the preamplifier and latch combination is 2.25 V/V. The comparator then drives an SR-latch

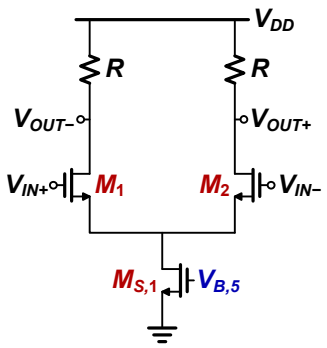


Figure 5.26: Preamplifier for the summing comparator.

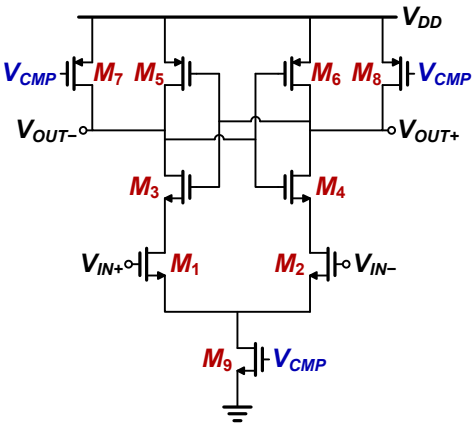


Figure 5.27: Latch for the summing comparator.

that generates full-logic levels for the D/A converter.

The latch mode time constant τ_L and offset delay t_o are found by simulating the latch time for progressively smaller inputs through the preamplifier and latch combination. Referring to Fig. 5.28, τ_L =38 ps and t_o =107 ps where τ_L is the time constant associated with the slope of the line, and t_o is the minimum delay for the latch when the input voltages are large.

Metastability can be a problem if the latch does not resolve a small input in the allotted time. Assuming the output needs to be resolved in about 450 ps based on the non-overlap time of the two-phase clocks, the probability of an error is equal to the probability that the output of the latch is less than about 0.9 V (enough to trigger the subsequent stage) [78].

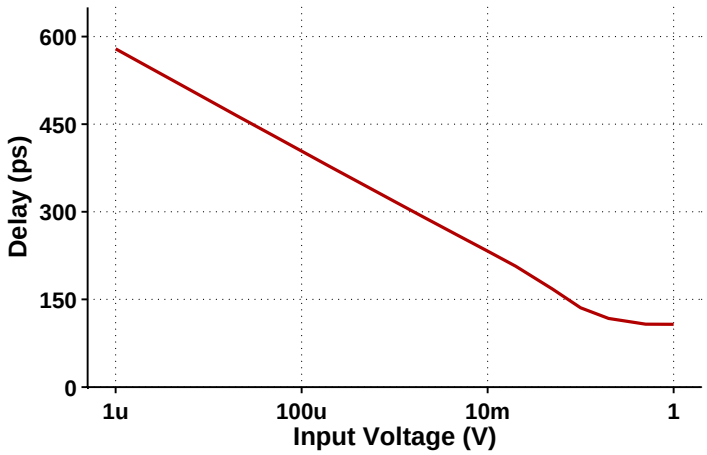


Figure 5.28: Simulation for finding latch mode time constant.

The output of the latch after 450 ps is

$$V_{OUT} = 2.25V_{IN}e^{(t-t_o)/\tau_L} = 2.25V_{IN}e^{9.0}. \tag{5.28}$$

The probability of an error is

$$P_{error} = P(|2.25V_{IN}e^{9.0}| < 0.9) = P(|V_{IN}| < 49.4\,\mu\text{V}). \tag{5.29}$$

Since V_{IN} is assumed to be uniformly distributed between -0.4 V and 0.4 V, the probability that it is less than 49.4 µV is 1 in 8100. This is much better than the required converter accuracy as the error is at 78.2 dB below full-scale (note that this error is significant because it results in a D/A converter error and appears at the input of the converter).

5.3.2 Digital-to-Analog Converter

The 3-level D/A converter signal is created by splitting the sampling capacitor into two parallel sections, as shown in Fig. 5.29. The SR-latch from the A/D converter controls a tri-state inverter with reference voltages of $V_L = 0.5\,\text{V}$ and $V_H = 1.3\,\text{V}$ that provide the desired reference voltage for the sampling capacitor on phase ϕ_2.

When the reference voltages V_H and V_L have a non-zero impedance, the current injected into the circuit from these references is signal-dependent since the D/A capacitor is shared

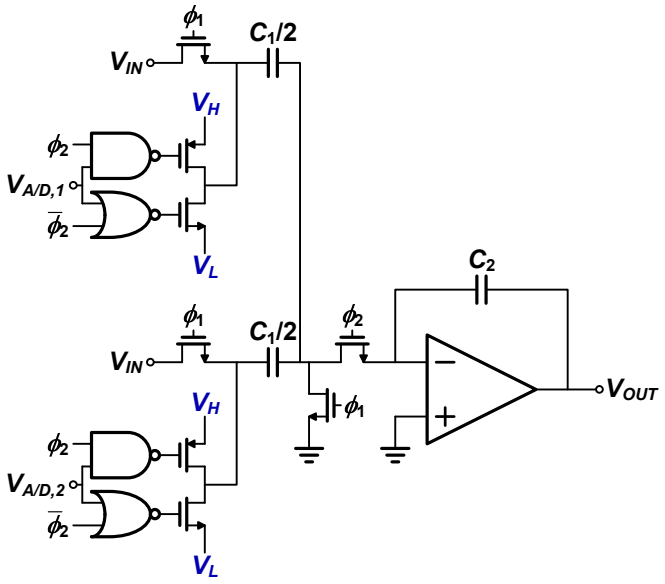


Figure 5.29: D/A converter voltages control two separate branches at the input of the integrator.

[79]. For this reason, extra care was taken to keep this impedance low. When a separate D/A converter capacitor is used, the linearity is improved since the current is no longer signal dependent, but this comes at the cost of increased thermal noise, resulting in increased power. The trade-off was made based on the assumption that a reference voltage could be found with a low enough output impedance.

5.3.3 Switches

Fig. 5.30 shows the eight distinct switches used in the integrator stages. Switches S_3-S_6 are attached to the OTA virtual ground node, passing voltages of 0.4 V (the input common-mode voltage). Simple NMOS transistors are sufficient for these switches.

Switch S_2 is the D/A converter switch and was discussed in Section 5.3.2. Switches S_1, S_7 and S_8 are implemented as transmission gates since they pass a signal with a common-mode voltage of 0.9 V (S_7 should have no signal on it, but a transmission gate is still necessary for reduced impedance). Switch S_1 is bootstrapped at the first stage input, and bottom-plate sampling is used on every stage.

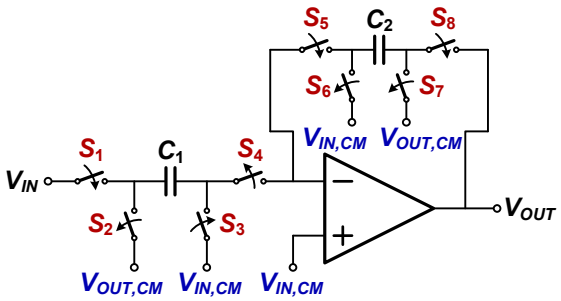


Figure 5.30: Eight separate switches of the integrator stages. While there are more switches from the two-phase resetting scheme and the separate input branch from the D/A converter, they only replicate the eight switches shown here.

Bootstrapping

Every sampling switch in the switched-capacitor data converter samples a discrete-time signal, except for the input switch which samples a continuous-time signal. With a discrete-time signal, it is only necessary that the time constant of the switch on-resistance R_{ON} and the sampling capacitor is small enough for settling within the sampling period. However, for a continuous-time signal, the time constant must be small and the variation in R_{ON} must also be sufficiently low as the input signal varies. The on-resistance R_{ON} of an NMOS sampling switch in the triode region is equal to

$$\begin{aligned} R_{ON} &= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - Vt)} \\ &= \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{IN} - Vt)}. \end{aligned} \tag{5.30}$$

Since V_G is equal to the clock high voltage V_{DD}, and V_S is dependent on the input signal V_{IN}, V_{GS} varies depending on the input signal amplitude. For this reason, special care must be taken for the input sampling switch, and bootstrapping is often necessary to reduce the variation in R_{ON}.

The bootstrapped circuit is shown in Fig. 5.31 for an NMOS sampling switch [80]. On ϕ_2 the capacitor C_B is charged to the supply voltage V_{DD}. Also, the gate of the sampling switch M_S is grounded to turn it off. On ϕ_1 the capacitor C_B is connected between the input and the gate of the sampling switch M_S, which keeps the transistor V_{GS} at approximately V_{DD}. The strength of transistor M_5 is responsible for how quickly the sampling switch turns

off, while transistors M_1 and M_4 determine how quickly the sampling switch turns on.

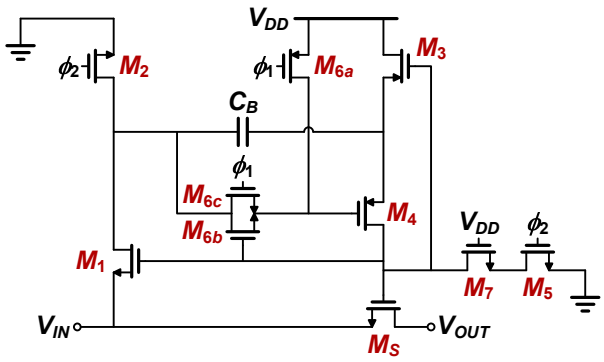


Figure 5.31: Bootstrapping circuit for sampling transistor M_S.

The V_{GS} of the sampling switch M_S will be less than V_{DD} because of charge sharing between C_B and the gate-source capacitance of M_S. The resulting gate voltage of M_S is

$$V_G = (V_{IN} + V_{DD}) \frac{C_B}{C_B + C_{GS}} \tag{5.31}$$

while the source voltage is V_{IN}. It is important to ensure that C_B is significantly larger than C_{GS} to ensure a large V_{GS}. In this design, C_B was kept ten times larger than C_{GS}.

Additional care must be taken to ensure some nodes in the circuit do not exceed the allowable V_{GS} of their respective transistors. Transistors M_{6a}, M_{6b} and M_{6c} control the gate voltage of M_4 without overstressing its V_{GS}. Transistor M_7 keeps the V_{GD} of M_5 from reaching $2V_{DD}$ [80]. Also, the gate of M_3 is tied to the gate of M_S to turn it off during ϕ_1.

Bottom-Plate Sampling

Although not explicitly shown in the previous figures, all integrators have employed bottom-plate sampling for the switches, as shown in Fig. 5.32 [63, 81]. Advanced clocking is used on all switches attached to the virtual ground node (switches S_3-S_6). This ensures that the charge injected into the respective capacitors is signal independent as it only relies on the voltage at DC bias nodes. Signal dependent charge would normally be injected from switches S_1, S_2 and S_8 since each of these switches has a side connected to a signal-dependent voltage signal. Since the sampling takes place on the advanced clock phase

(using switches S_3, S_4 and S_5, respectively), the signal-dependent charge does not impact the final voltage.

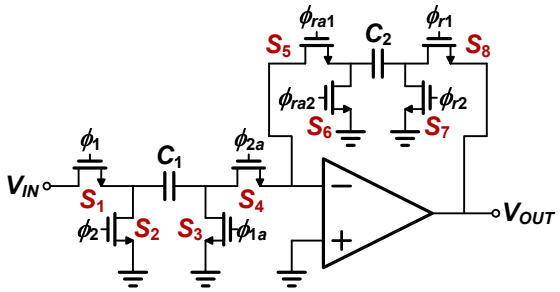


Figure 5.32: Bottom-plate sampling using an advanced clock on switches S_3 to S_6.

5.3.4 Clock Generator

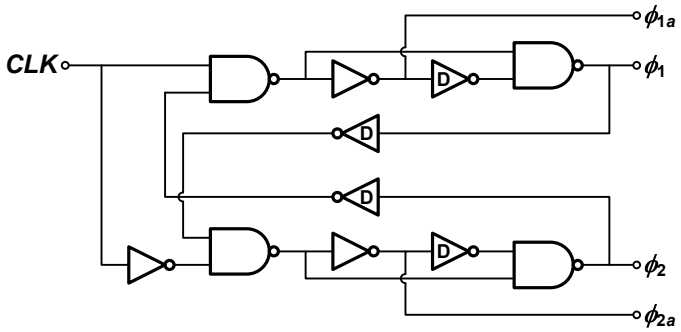
Non-Overlapping Clocks

The non-overlapping clock generator was designed to generate two non-overlapping clocks, as well as two advanced non-overlapping clocks for bottom-plate sampling. The schematic is shown in Fig. 5.33. The non-overlap time and the advanced clock falling edge are adjusted by adding pairs of inverters to the single inverters labeled 'D' in Fig. 5.33. The advantage of this circuit is that the rising edge of the advanced clock aligns with the typical rising edge, maximizing the time available for settling within the sampling period.

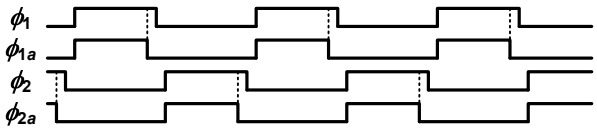
Three inverters were used in both the feedback path as well as the forward path so that the resulting non-overlap time and advanced clock time were 470 ps and 430 ps, respectively. These values were obtained by measuring the time between falling and rising edges at 10 % of V_{DD} (180 mV) on the slow corner.

Clock Divider and Reset Signals

To generate the appropriate reset phases for the incremental A/D converter the clock signal is divided by 3 (for an OSR of 3), or 1 (for the pipeline mode). A third option where the reset phases are held is also required for the $\Delta\Sigma$ mode. Fig. 5.34 shows the divider using negative edge-triggered D flip-flops with the appropriate control switches S_0, S_1 and S_3 for their respective OSRs of 0 (infinity), 1 and 3.



(a) Clock Generator



(b) Advanced Clocking Scheme

Figure 5.33: Non-overlapping clock generator with advanced clocking scheme.

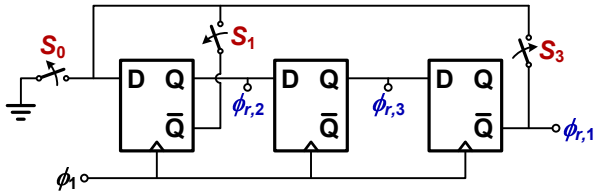


Figure 5.34: Clock divider for an incremental A/D converter with operation at an OSR of 1, 3 or infinity.

In the incremental mode (OSR of 3) the reset clocks $\phi_{r,1}$, $\phi_{r,2}$ and $\phi_{r,3}$ generated with this clocking scheme have a 50 % duty cycle. They must be adjusted slightly so that they can switch the two integrating capacitors between the time when ϕ_1 falls and ϕ_2 rises. The circuit used to accomplish this is shown in Fig. 5.35. When ϕ_2 rises and $\phi_{r,1}$ is high, the output $\phi_{r,1o}$ turns on and the lower branch is activated until ϕ_1 is low and $\phi_{r,1}$ falls. The same circuit is used to generate $\phi_{r,1e}$ where the reference reset clock is $\overline{\phi_{r,1}}$ instead of $\phi_{r,1}$ (and similarly for the rest of the reset clocks $\phi_{r,2o}$, $\phi_{r,2e}$, $\phi_{r,3o}$, $\phi_{r,3e}$).

When operating in the pipeline mode (OSR of 1), the clock divider of Fig. 5.34 and the non-overlapping reset clock generator of Fig. 5.35 both generate the appropriate non-overlapping reset clocks when S_1 (of Fig. 5.34) is enabled. There is no difference between the three phases $\phi_{r,1}$, $\phi_{r,2}$, and $\phi_{r,3}$ (aside from inversions), and therefore the order of them

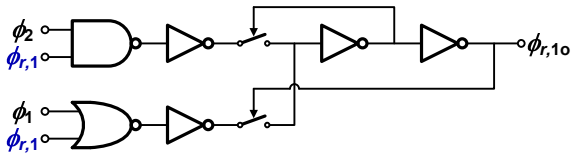


Figure 5.35: Non-overlapping reset clock generator.

relative to each other does not matter.

The ΔΣ mode is even simpler because no resetting is required. The three flip-flops of Fig. 5.34 are either on or off and do not change values. Therefore, the non-overlapping reset clock generator simply passes the zero value generated by the clock divider for $\phi_{r,1}$, $\phi_{r,2}$, and $\phi_{r,3}$.

Clock Driver

While all the previous gates used small unit-sized inverters with 1 µm/0.18 µm NMOS devices and 3 µm/0.18 µm PMOS devices, the clock drivers are much larger to drive the capacitive loads of both the switches and the long clock lines. One clock driver is shown in Fig. 5.36 with the sizes relative to a unit-sized inverter. Due to the size of the large clock drivers, the total digital power dissipated in the clocks is 20.6 mW.

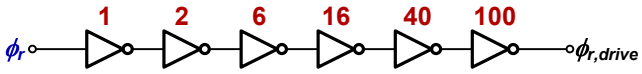


Figure 5.36: Clock driver with sizes relative to a unit-sized inverter (1 µm/0.18 µm NMOS and 3 µm/0.18 µm PMOS).

5.3.5 Analog Multiplexer

To test the data converter at low frequencies an analog multiplexer is used to probe various DC nodes (as well as some moving signals). The analog multiplexer was designed to only operate on slow moving signals since minimum-sized devices are used to pass the signals. A total of 46 nodes can be probed with the multiplexer.

A single control signal (generated serially through a shift register) activates two multiplexer outputs. The individual analog multiplexer cells include a local transmission gate with a pull-up PMOS transistor to either probe the node voltage or disconnect from it. The

PMOS transistor pulls the disconnected node high to avoid coupling any signal to the long wire connecting the probe to the selector circuit. A transmission gate on the selector side is also used to connect or disconnect the probed node. The multiplexer is shown in Fig. 5.37.

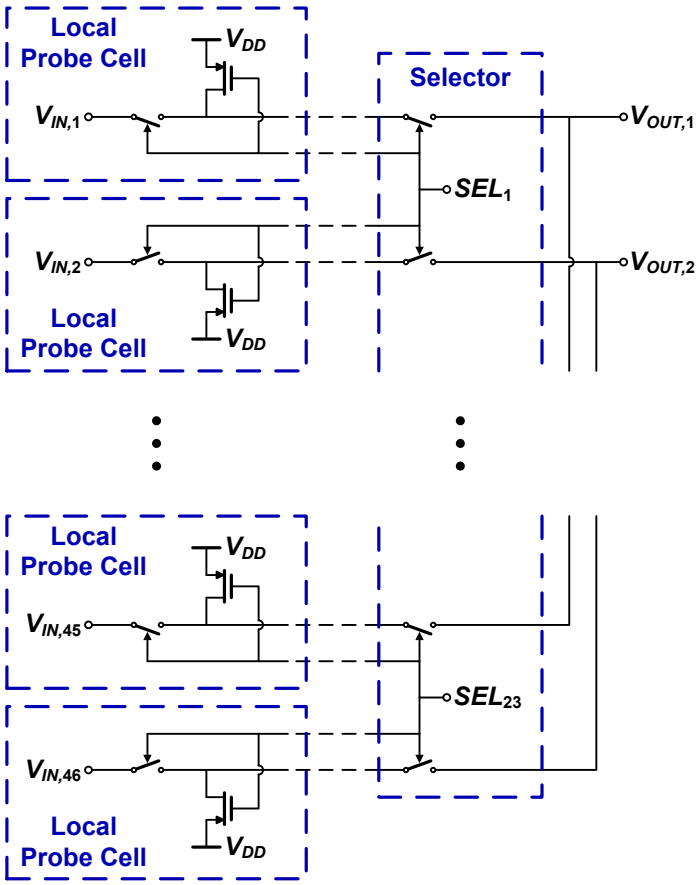


Figure 5.37: Analog multiplexer with two local probe cells for each selector portion of the circuit. Each output node is tied to 23 parallel multiplexer cells, resulting in 23 selector signals from 23 shift registers.

5.3.6 Layout

Three distinct stages were designed as scaled versions of each other. The layout was similar to a pipeline A/D converter where the 8 stages were lined up as scaled slices of each other. Special care was taken in a few areas, as discussed below.

Capacitors

The sampling and integrating capacitors were designed to match each other in each of the individual stages. A common-centroid layout was used to ensure optimal matching. The pattern used to match these four equally sized capacitors is shown in Fig. 5.38.

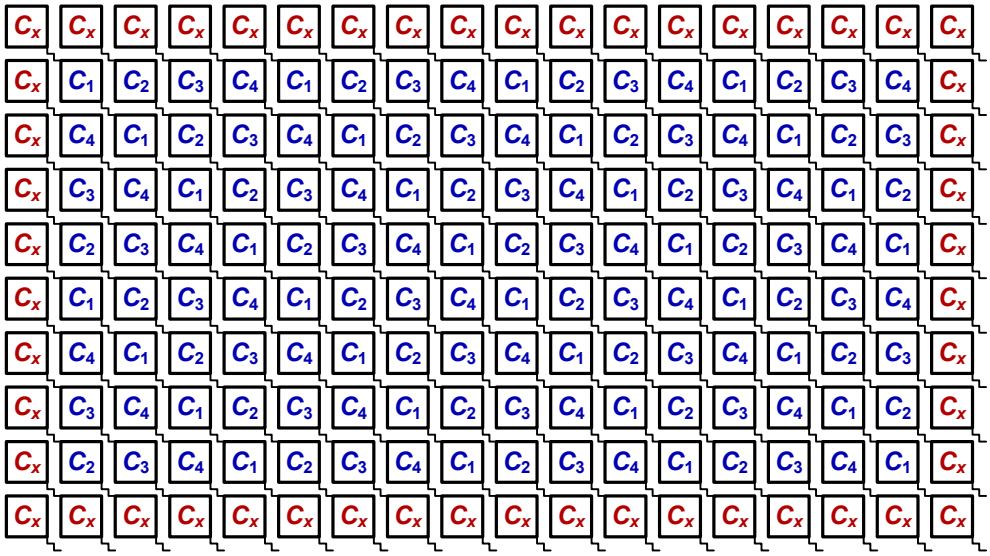


Figure 5.38: Common-centroid layout pattern for four capacitors with additional dummy capacitors C_x.

Biasing

A master bias circuit was designed on the lower side of the chip. Currents are passed to each of the OTAs, and each one generates its own bias voltages with its respective bias circuits. While these circuits are all identical for each OTA (since the OTAs are simply scaled versions of each other), local bias generation is used to minimize the IR drop and potential mismatch in V_{GS} values. The disadvantage of this choice is that the local bias in each stage consumed constant power regardless of the stage size. As shown in Table 5.7, 3.4 mW is dissipated in every stage resulting in a total of 30.2 mW dedicated to biasing the stages of the data converter.

5.4 System Simulations

Simulations were performed on the entire system to ensure proper operation before fabrication. The pipeline A/D converter, 8-stage cascaded ΔΣ modulator, and incremental data converter were simulated to ensure proper operation on the typical corner. Additionally, simulations of the incremental data converter were performed on the slow and fast corners. These simulations were performed without thermal noise.

The simulation results are summarized in Table 5.6. A minimum of 64 in-band bins were obtained in each simulation, and a sample output spectrum of the incremental data converter is shown in Fig. 5.39 where the SNDR is 75.9 dB. Output spectrums of the pipeline data converter as well as the ΔΣ modulator are shown in Fig. 5.40 and Fig. 5.41, respectively. A final simulation of the incremental data converter with parasitic capacitor extraction is also included in Table 5.6 where capacitors below 1 fF were removed.

Architecture	Sampling Frequency	Signal Bandwidth	OSR	Corner	SNDR
Incremental	100 MHz	16.7 MHz	3	TT	75.9 dB
Incremental	100 MHz	16.7 MHz	3	SS	75.1 dB
Incremental	100 MHz	16.7 MHz	3	FF	75.4 dB
Incremental	100 MHz	16.7 MHz	3	SF	78.3 dB
Incremental	100 MHz	16.7 MHz	3	FS	73.4 dB
Pipeline	100 MHz	50 MHz	1	TT	50.3 dB
Cascaded ΔΣ	100 MHz	16.7 MHz	3	TT	67.4 dB
Incremental (Extracted)	100 MHz	16.7 MHz	3	TT	72.3 dB

Table 5.6: Transistor-level A/D converter simulations for the three different architectures without thermal noise.

Table 5.7 lists the power consumed for each circuit of the incremental data converter, broken down by stage. A power breakdown is also included for the individual circuits of stages 1, 2 and 4 since these are the three distinct stages in the design.

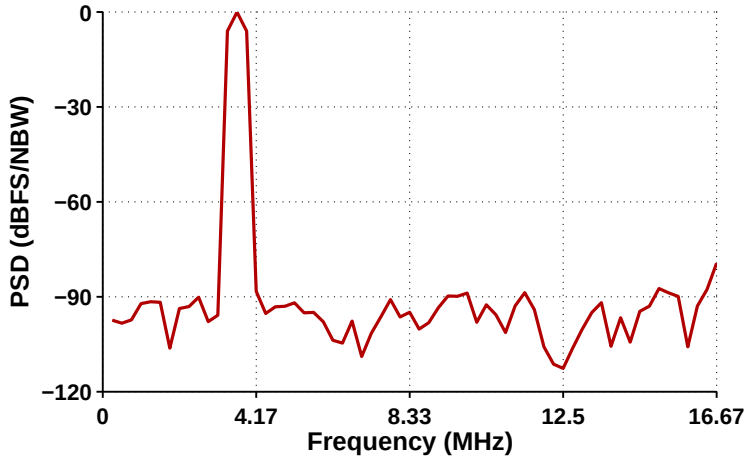


Figure 5.39: Simulated output spectrum for the 8th-order incremental A/D converter (NBW = 391 kHz). The SNDR is 75.9 dB.

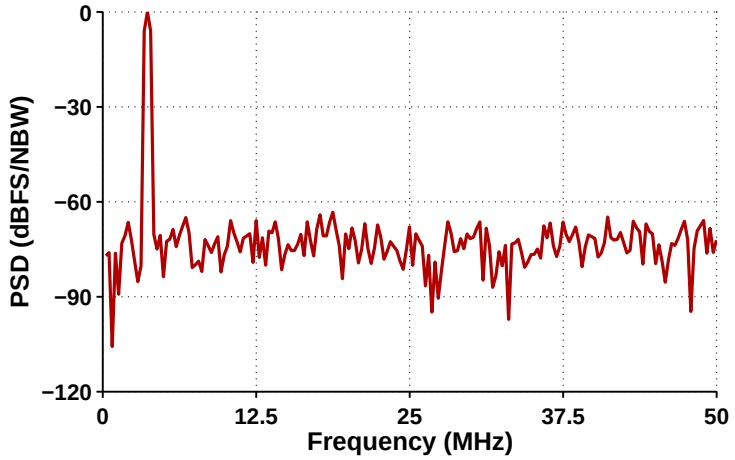


Figure 5.40: Simulated output spectrum for the 8-stage pipeline A/D converter (NBW = 391 kHz). The SNDR is 50.3 dB.

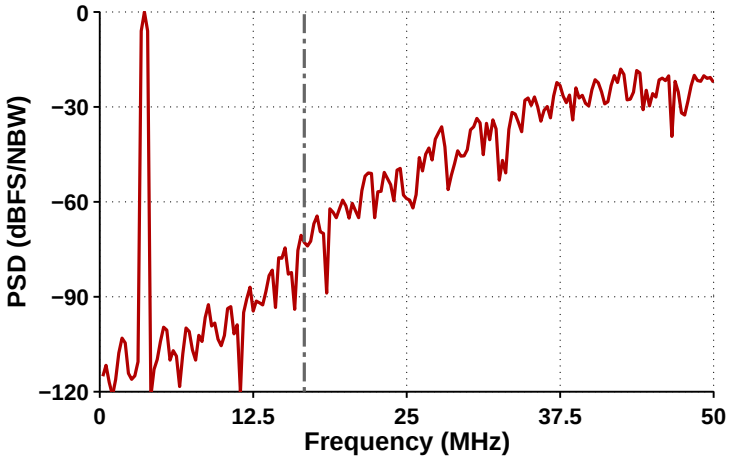


Figure 5.41: Simulated output spectrum for the 8th-order cascaded ΔΣ modulator (NBW = 391 kHz). The SNDR is 67.4 dB.

Block	Circuit	Power
Stage 1	OTA	24.0 mW
Stage 2,3	OTA	12.0 mW
Stage 4-8	OTA	3.0 mW
Stage 1	Gain-Boosters	13.0 mW
Stage 2,3	Gain-Boosters	7.0 mW
Stage 4-8	Gain-Boosters	3.2 mW
Stage 1-8	Comparators	0.5 mW
Stage 1-8	Local Bias	3.4 mW
Stage 1	All	40.9 mW
Stage 2,3	All	22.9 mW
Stage 4-8	All	10.1 mW
Global Bias	All	3.0 mW
Clocks/Digital	All	20.6 mW
Total		160.7 mW

Table 5.7: Power breakdown of the 8th-order incremental data converter at a sampling frequency of 100 MHz.

Chapter 6

Experimental Results

The 8-stage A/D converter discussed in Chapter 5 (Fig. 5.1) was fabricated in 0.18 µm CMOS technology. This chapter presents the experimental results obtained from the test chip. The chip was tested as a pipeline A/D converter, a cascaded ΔΣ modulator, and an incremental data converter. The test setup will be described in Section 6.1, and the remaining sections will discuss the results from each mode of operation.

6.1 Test Setup

6.1.1 Fabricated Chip

A chip micrograph is shown in Fig. 6.1 where the 8 distinct stages are highlighted, as well as the clock generator. The active area is 2.7 mm by 1.0 mm. Decoupling capacitors cover the unused chip area.

6.1.2 Printed Circuit Board

The chip was packaged in a 44-pin *ceramic quad flat pack* (CQFP). A custom 4-layer *Flame Retardant 4* (FR-4) *printed circuit board* (PCB) was designed to test the 44-pin CQFP. On the PCB the input is passed through a single-ended to differential transformer where the output common-mode of the differential signal can be easily adjusted by adjusting the common node on the transformer. Voltage references are generated for six voltages: the quantizer high and low reference voltages, the D/A converter high and low reference

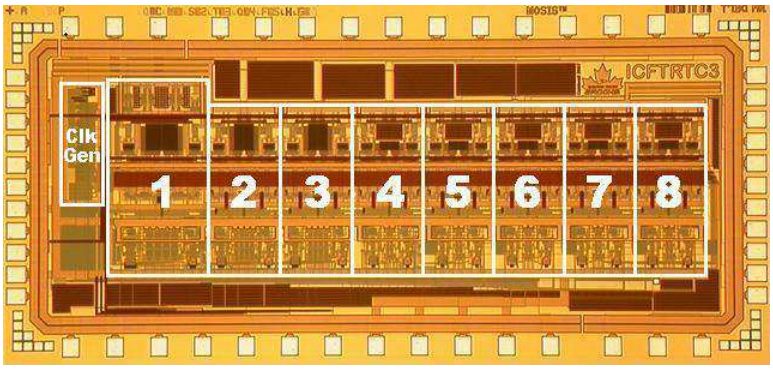


Figure 6.1: Chip micrograph. The active area is 2.7 mm by 1.0 mm.

voltages, and the input and output common-mode voltages. A crystal oscillator is on-board to produce a cleaner clock signal, as well as the option for an external clock generator. Buffers are used on the digital outputs to drive the logic analyzer. Data is shifted into the chip from a parallel port of a computer to adjust some settings, including the converter mode of operation and the chosen analog multiplexer output. A PCB photo is shown in Fig. 6.2.

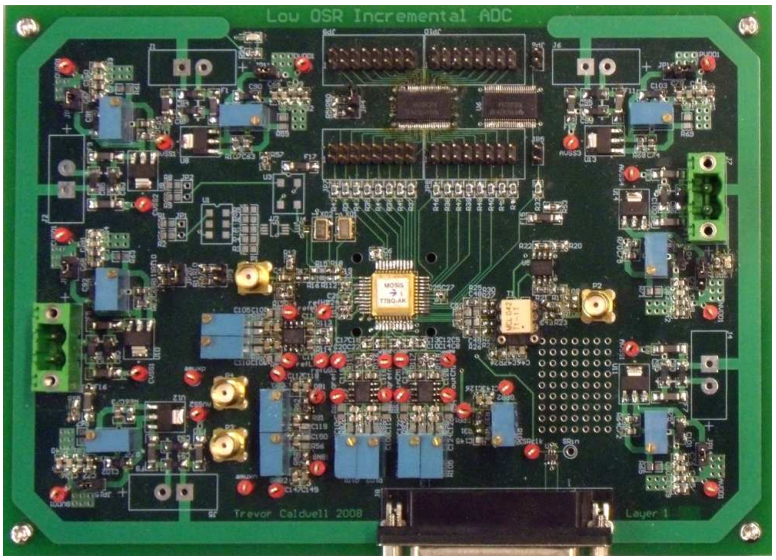


Figure 6.2: 4-layer PCB photo (178 mm by 127 mm).

The 4-layers of the PCB are divided as follows: signal routing on the top layer, ground

planes on the second layer, power planes on the third layer, and more signal routing on the bottom layer. The ground plane is divided into three separate planes for the clock/crystal oscillator ground, the digital output/buffer ground, and the analog ground. The power plane is divided into five separate planes. These planes are similar to the division of the ground planes. The clock/crystal oscillator power plane is divided into two separate planes due to the different voltage requirements of the various crystal oscillators that are available on the PCB. Also, the analog power plane is separated into two planes, one for the voltage references, and the other for the analog power to the chip.

6.1.3 Equipment

The equipment setup surrounding the PCB is shown in Fig. 6.3. The Rohde & Schwarz SMT03 signal generator is used to generate a single-ended sinusoidal signal that is converted to a differential signal on the PCB with a transformer. A Mini-Circuits low-pass filter is used to maintain low distortion on the input signal fed to the PCB (specific cut-off frequencies were available and the chosen input signal frequencies reflect these cut-off frequencies).

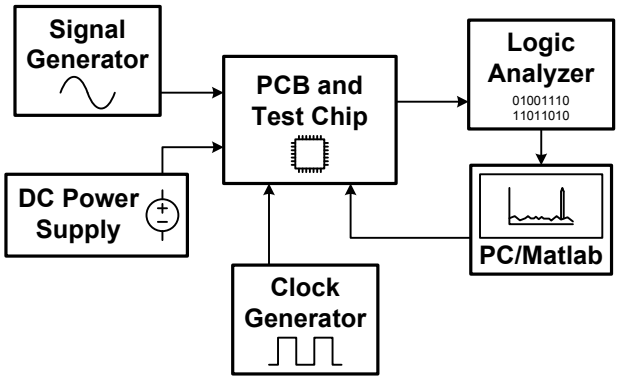


Figure 6.3: Equipment test setup surrounding the PCB and test chip. The PC controls the various settings of the test chip.

An Agilent E3620A DC power supply is used to generate a single voltage supply that is used for the entire PCB. The PCB then generates the individual voltage sources necessary for all power and ground planes from this power supply. The voltage used is 6 V, and an alternative to the Agilent E3620A DC power supply is simply a set of four 1.5 V batteries.

The Wavetek 395 Arbitrary Waveform Generator is used as a clock generator. It provides a single-ended clock with a 0 V common-mode voltage which is AC coupled on the board with a DC bias of 0.9 V, resulting in the expected 0 V to 1.8 V clock signal. An alternative to the clock generator is the on-board crystal oscillator. Both were tested with negligible differences between the two.

The NCI GoLogic Analyzer is used for data collection. It is a PC-based logic analyzer. The data is collected within the logic analyzer and passed to the PC where Matlab is used to evaluate the output. Matlab is also used to set the mode of operation and the settings for the analog multiplexer (adjusting the settings before the data is captured). This allows various nodes on the test chip to be probed with either an oscilloscope or a digital multimeter (not shown in Fig. 6.3).

6.2 Pipeline Mode

When operated as an 8-stage 1.5 bit/stage pipeline A/D converter, the expected SNDR is 50 dB. This is because the maximum attainable SQNR is 50 dB, and the thermal noise floor is low enough at -72 dB that it does not significantly affect the overall resolution.

The data converter output in the pipeline mode is slightly different than a typical pipeline converter because of the absence of a low-resolution (2-bit) flash A/D converter on the last stage output. Also, the standard operation of the converter maintains the same reference voltages for the D/A converters and comparators as used in the incremental mode. Therefore, the error signal shown in Fig. 2.14 does not accurately represent this particular pipeline converter (although it could if the reference voltages were adjusted), and the actual error signal is as shown in Fig. 6.4. This architecture is not as resilient as the standard pipeline architecture to distortion resulting from comparator offset (as described in Section 2.3.2), but simulations indicated that with some margin in the OTA output swing, this should not be a problem. Redundancy is still present as each stage has 3 output levels for 1 bit of resolution, so errors causing incorrect outputs can still be corrected by later stages. The resulting expected resolution of this 8-stage 1.5 bit/stage architecture is 8 bits (or 50 dB).

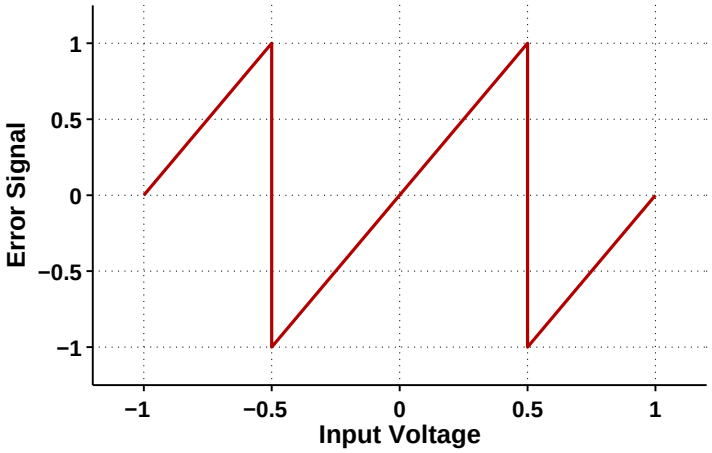


Figure 6.4: Pipeline stage error signal using the same reference voltages as those in the incremental mode.

6.2.1 Bias Voltages

To ensure proper biasing of the pipeline A/D converter (and all other modes since the biasing is the same), the DC bias voltages were measured. With three unique OTA designs on the chip (which were all scaled versions of each other), three sets of bias voltages for the main OTA and the gain-boosters were measured (from the first, second and fourth stages). They are compared to the expected values based on simulations on the typical corner, as summarized in Table 6.1.

The results suggest that the chip was not fabricated on a typical corner. Further simulations show that the chip is more likely towards the slow (SS) corner. Both PMOS and NMOS generated bias voltages are between the typical and slow values. These results are summarized in Table 6.2 for the first stage (due to the similarity between the voltages in stage 1, 2 and 4 in Table 6.1, only stage 1 results are compared).

6.2.2 Static Testing

The output versus input transfer function of the pipeline A/D converter was measured at a sampling frequency of 50 MHz. The entire input range was swept with a DC input signal to construct a staircase output. The histogram-based *integral non-linearity* (INL)/DNL test is another way to infer the output versus input of a pipeline A/D converter, but it was not

		Bias Voltages (mV)					
		Stage 1		Stage 2		Stage 4	
Block	Node	Sim.	Meas.	Sim.	Meas.	Sim.	Meas.
Main OTA	$V_{B,1}$	662	763	662	775	662	784
	$V_{B,2}$	1021	1097	1021	1097	1021	1112
	$V_{B,3}$	782	731	782	735	782	720
	$V_{B,4}$	1156	1074	1156	1069	1156	1069
Gain-Booster A_P	$V_{B,1}$	662	760	662	766	662	780
	$V_{B,2}$	1021	1078	1021	1082	1021	1106
	$V_{B,3}$	782	739	782	738	782	735
	$V_{B,4}$	1156	1071	1156	1071	1156	1069
	$V_{B,6}$	1046	980	1046	976	1046	973
Gain-Booster A_N	$V_{B,1}$	670	757	670	760	670	767
	$V_{B,2}$	1033	1071	1033	1085	1033	1095
	$V_{B,3}$	782	743	782	738	782	737
	$V_{B,4}$	1156	1073	1156	1068	1156	1065
	$V_{B,5}$	636	733	636	749	636	755

Table 6.1: Simulated and measured bias voltages for the OTAs and gain-boosters from the first, second and fourth stages. Simulated results are taken from the TT corner at 80 °C.

used since it does not fully disclose the static behaviour in the presence of a non-monotonic output code (for example, due to gain errors). The histogram-based test assumes that a full-scale sinusoidal input should have a known distribution across the digital output bins. When the resulting digital output distribution deviates from the expected distribution, the increase/decrease of each bin count represents a widening/narrowing of those bins. The DNL and INL error can then be inferred from these results. When gain errors are present, the output code may have discontinuities. The histogram-based method only counts the number of outputs for each digital code, and ignores when they occurred. A sample is shown in Fig. 6.5. The two cases shown will have identical distributions in a histogram-

Block	Node	Stage 1 Bias Voltages (mV)		
		Simulated TT	Measured	Simulated SS
Main OTA	$V_{B,1}$	662	763	765
	$V_{B,2}$	1021	1097	1089
	$V_{B,3}$	782	731	680
	$V_{B,4}$	1156	1074	1039
Gain-Booster A_P	$V_{B,1}$	662	760	765
	$V_{B,2}$	1021	1078	1089
	$V_{B,3}$	782	739	680
	$V_{B,4}$	1156	1071	1039
	$V_{B,6}$	1046	980	878
Gain-Booster A_N	$V_{B,1}$	670	757	767
	$V_{B,2}$	1033	1071	1052
	$V_{B,3}$	782	743	680
	$V_{B,4}$	1156	1073	1039
	$V_{B,5}$	636	733	748

Table 6.2: Stage 1 simulated and measured bias voltages on both the TT and SS corners at 80 °C. The measured results indicate that the test chip was fabricated between the typical and slow corners.

based INL/DNL plot, and the potential to overlook the gain error exists, especially if the input sinusoid is fast enough that it does not exercise every code sequentially, causing the output to appear monotonic.

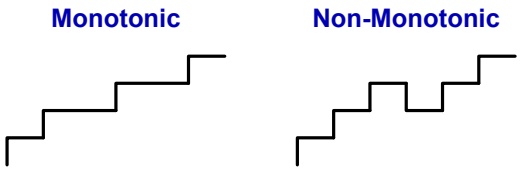


Figure 6.5: Two output codes that give the same histogram when using a histogram based INL/DNL measurement.

Output vs. Input

A portion of the output versus input transfer function is shown in Fig. 6.6. The discontinuity in the output code indicates a gain error is present which can be calibrated out with a gain adjustment to the second *most significant bit* (MSB) code.

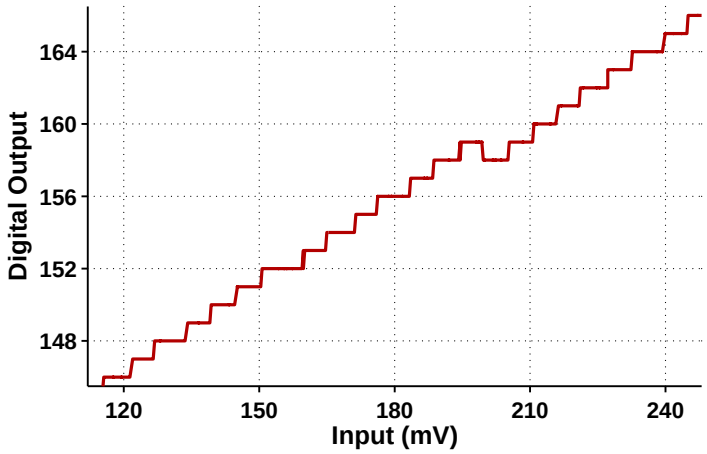


Figure 6.6: Portion of the output versus input curve for the pipeline A/D converter with a gain error.

The transition points are less precise than would be typically expected due to mismatches between the two integrating capacitors C_{2o} and C_{2e} on different phases (see Fig. 5.2). With slightly different values, every second sample will have a slightly different transfer function and transition points. As an example of the different transitions, the two digital outputs from alternating phases are separated and shown in Fig. 6.7. This was one of the concerns with the chosen clocking scheme but it was assumed that the capacitors could be matched to a sufficient level of accuracy to avoid this problem. At the 8-bit level this is a reasonable assumption, but for the desired 12-bit resolution of the incremental data converter this is not sufficient.

DNL and INL Error

The DNL and INL error were evaluated after gain error calibration at a sampling frequency of 50 MHz. The input was gradually swept so that an average of about 10 inputs were collected for every digital output level. The transition point was then estimated based on

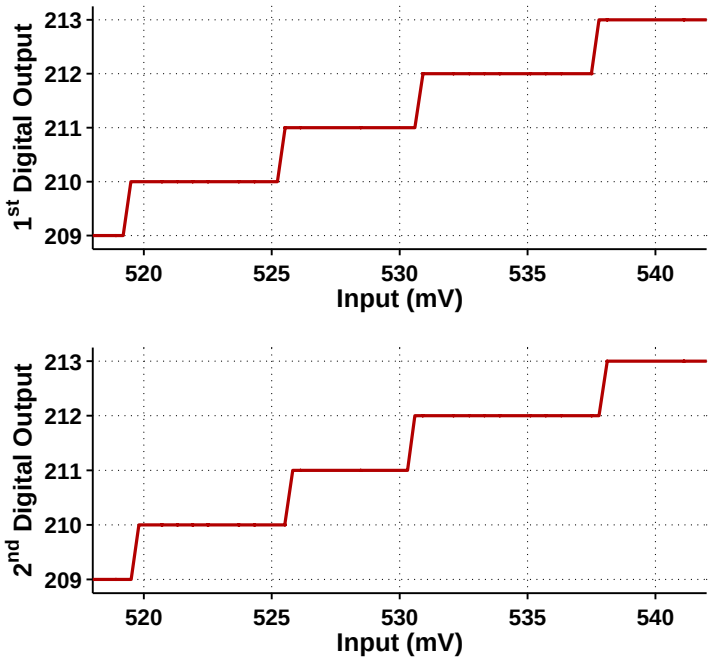


Figure 6.7: Differing transition points of the two outputs on alternating phases of the pipeline A/D converter.

the number of occurrences of each output level for the different input voltages. The DNL error is shown in Fig. 6.8 and is between -0.40 LSB and +0.39 LSB. The INL error has a maximum of +0.97 LSB and a minimum of -0.80 LSB as shown in Fig. 6.9.

6.2.3 Dynamic Testing

The pipeline A/D converter was also tested with a sinusoidal input at a sampling frequency of 50 MHz. A sample *fast Fourier transform* (FFT) is shown in Fig. 6.10 with a full-scale input and an SNDR of 43.1 dB and an *signal-to-noise ratio* (SNR) of 48.4 dB with an input signal at 1.9 MHz. Many spurs appear in the output as a result of non-linearities that are also present in the incremental A/D converter and are discussed in Section 6.5. Gain calibration does not improve the SNDR since the error is dominated by these non-linearities.

The input frequency was swept between DC and 20 MHz and the results are shown in Fig. 6.11. The resolution deteriorates at higher frequencies, but this is not unexpected

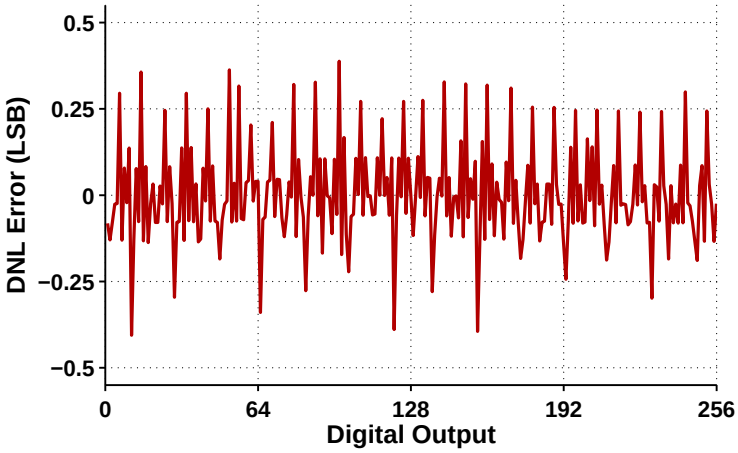


Figure 6.8: Differential non-linearity error.

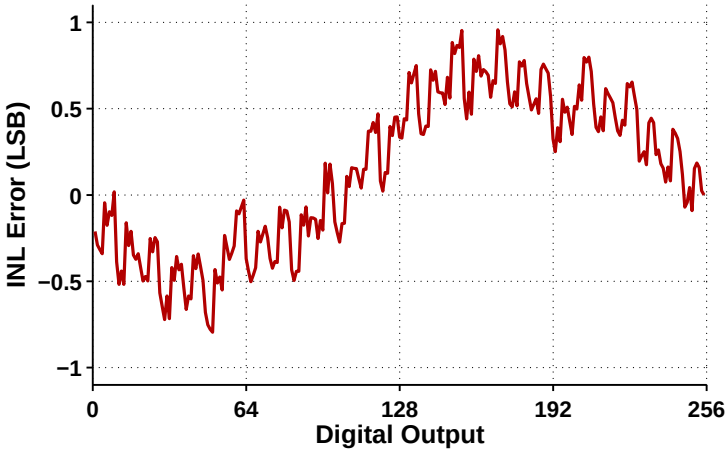


Figure 6.9: Integral non-linearity error.

because the pipeline converter does not have an input S/H. Mismatch in time constants of the two sampling networks at the input (the sampling switch and the comparator) can cause aperture errors resulting in reduced dynamic performance at higher input frequencies [82].

The results for the pipeline A/D converter are summarized in Table 6.3. The pipeline A/D converter power is higher than it should be since the entire converter is oversized for the lower noise floor of the incremental data converter.

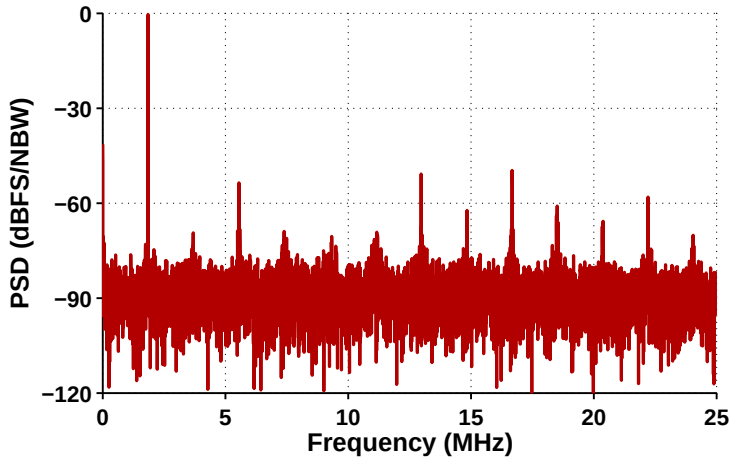


Figure 6.10: Output spectrum for the 8-stage pipeline A/D converter with an input at 1.9 MHz (NBW = 4.6 kHz).

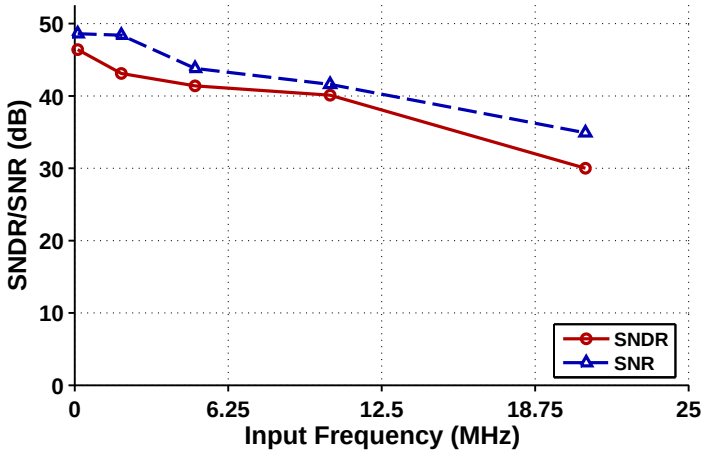


Figure 6.11: SNDR and SNR versus input frequency in the pipeline mode.

6.3 ΔΣ Mode

Once the pipeline A/D calibration was performed, the calibration code was used for the ΔΣ mode where the gain errors were calibrated but not the pole errors (see Eq. 4.11). The ΔΣ is an 8^{th}-order cascade of first-order stages and the peak SNDR achievable is 66 dB (ignoring any circuit non-idealities) since the thermal noise floor in this mode is at -72 dB, well below the SQNR (as with the pipeline A/D converter).

Parameter	Measured	Simulated
Sampling Frequency	50 MHz	50 MHz
Signal Bandwidth	25 MHz	25 MHz
SNDR (120 kHz)	46.4 dB	50.2 dB
SNR (120 kHz)	48.6 dB	N/A
SFDR (120 kHz)	53.5 dB	59.3 dB
Analog Power	135 mW	137 mW
Digital Power	16 mW	15 mW

Table 6.3: Summary of experimental results for the 8-stage pipeline A/D converter (simulated results do not include thermal noise).

Using a sampling frequency of 50 MHz the SNDR and SNR were evaluated at 2.1 MHz. The output spectrum is shown in Fig. 6.12. The second and third harmonics are in-band and the resulting SNDR and SNR are 60.1 dB and 61.3 dB, respectively. The SNR is not thermal noise limited since the thermal noise was designed to be 6 dB below the quantization noise.

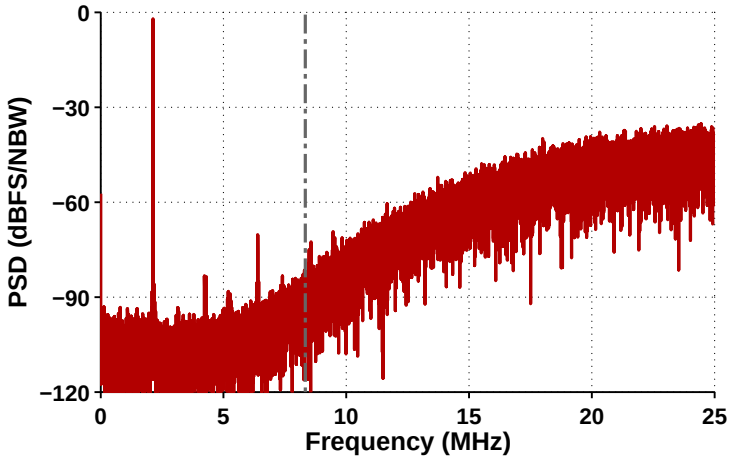


Figure 6.12: Output spectrum for the 8^{th}-order cascaded ΔΣ with an input at 2.1 MHz (NBW = 2.3 kHz).

The SNDR and SNR were measured for increasing input amplitudes and the results are shown in Fig. 6.13. The SNDR is 1.2 dB lower than the SNR at the peak. As expected, the

modulator is stable with full-scale inputs since the first stage is a 1st-order modulator.

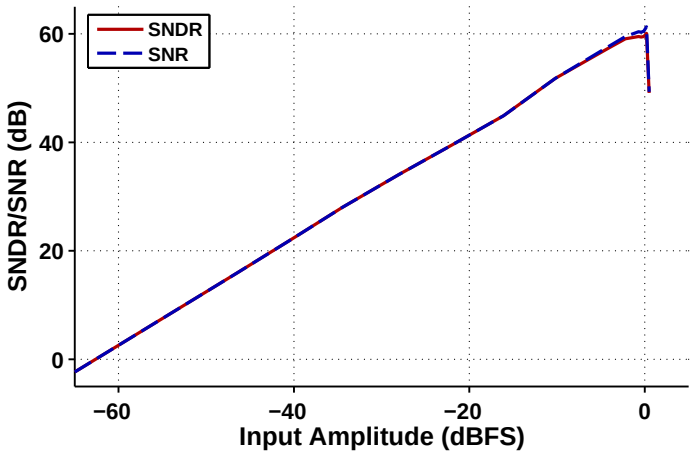


Figure 6.13: SNDR and SNR vs. Input Amplitude at an input frequency of 2.1 MHz. SNDR and SNR are similar and deviate by 1.2 dB at the peak.

The *effective number of bits* (ENOB) was also evaluated across various input frequencies as shown in Fig. 6.14. The resolution does not change by more than 0.2 bits as the input signal approaches the band edge at 8.33 MHz. At the higher input frequencies of 5.2 MHz and 8.3 MHz a two-tone test was used to keep the harmonics in-band for an accurate evaluation of SNDR (as opposed to SNR). When two tones are used, ENOB is defined slightly differently since the full-scale input must accommodate two tones that must be scaled so that they do not add up in phase and overload the modulator. With a single tone, ENOB is defined as [45]

$$\text{ENOB} = \frac{\text{SNDR} - 1.76}{6.02}. \tag{6.1}$$

When a two-tone signal is used the full-scale peak amplitude must remain the same, so the amplitude of each tone must be halved. The full scale signal power of the two tones is 3.01 dB less than a single tone. The resulting ENOB calculation is

$$\begin{aligned} \text{ENOB} &= \frac{\text{SNDR} + 3.01 - 1.76}{6.02} \\ &= \frac{\text{SNDR} + 1.25}{6.02}. \end{aligned} \tag{6.2}$$

The experimental results for the ΔΣ mode are summarized in Table 6.4, which includes

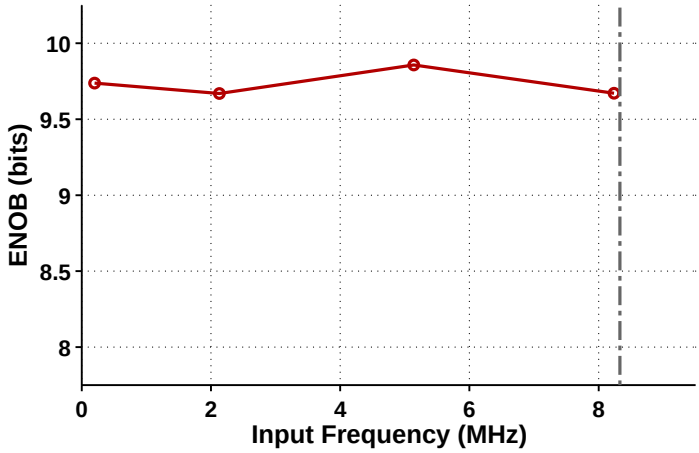


Figure 6.14: ENOB vs. Input Frequency. For the inputs at 5.2 MHz and 8.3 MHz, a two-tone measurement was made to ensure the harmonics were present in-band and added in the ENOB calculation.

the *spurious-free dynamic range* (SFDR). The results in this mode do not demonstrate a high power efficiency given the resolution and speed of operation. This is because the modulator has been oversized to operate in the incremental mode with a thermal noise floor well below that which is necessary for a 10-bit converter. Therefore the design has not been optimized for operation in the ΔΣ mode.

Parameter	Measured	Simulated
Sampling Frequency	50 MHz	50 MHz
Signal Bandwidth	8.33 MHz	8.33 MHz
SNDR (1.9 MHz)	60.1 dB	66.9 dB
SNR (1.9 MHz)	61.3 dB	N/A
SFDR (1.9 MHz)	66.1 dB	70.1 dB
Dynamic Range (1.9 MHz)	62.9 dB	—
Analog Power	95 mW	95 mW
Digital Power	14 mW	13 mW

Table 6.4: Summary of experimental results for the 8^{th}-order cascaded ΔΣ modulator (simulated results do not include thermal noise).

When compared to fully implemented low-OSR ΔΣ modulators, [11] attains a resolution of 50 dB at 20 MHz signal bandwidth in 76 mW, and [14] has a resolution of 73 dB at 10 MHz signal bandwidth in 240 mW. Both of these are 2-stage cascaded architectures with OSRs of 4, while this work is the first to push the OSR down to 3, and increase the number of cascaded stages to 8. While the power consumption is high, with a proper -62 dB thermal noise floor optimized for the ΔΣ mode, the power should decrease by roughly 10 times.

6.4 Incremental Mode

The incremental A/D converter was tested with a sinusoidal input at a sampling frequency of 50 MHz. A sample FFT is shown in Fig. 6.15. The SNDR is 39.9 dB and the SNR is 44.7 dB with a full-scale input signal at 4.9 MHz. Similar to the pipeline A/D converter, there are spurs in the output that indicate non-linear behaviour.

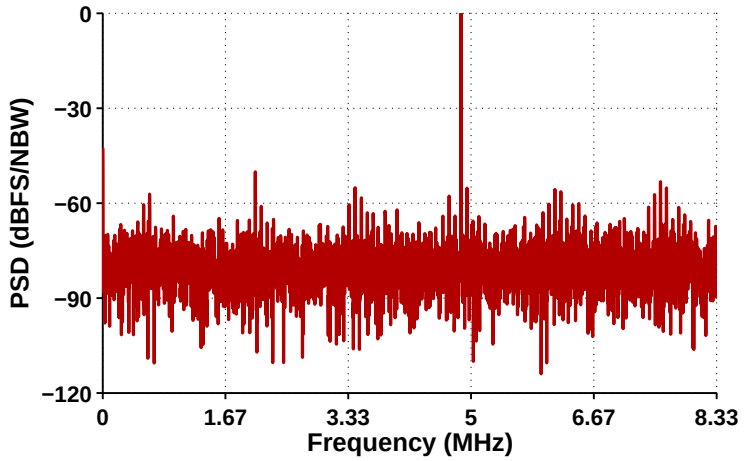


Figure 6.15: Output spectrum for the 8th-order cascaded incremental A/D converter with an input at 4.9 MHz (NBW = 3.1 kHz).

The input frequency was swept between DC and 4.9 MHz and the results are shown in Fig. 6.16. The resolution is relatively constant, although quite low due to the non-linearity present in the output. Unlike the pipeline A/D converter, the performance is not expected to deteriorate at higher frequencies despite not having an input S/H. This is because the input is oversampled and the input signal is 3 times slower.

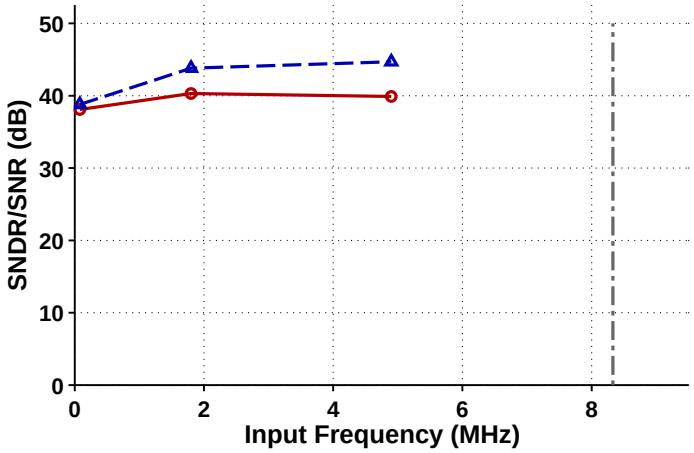


Figure 6.16: SNDR and SNR versus input frequency in the incremental mode.

The results for the incremental A/D converter are summarized in Table 6.5. The resolution is much lower than expected and the next section will discuss some potential pitfalls of the design.

Parameter	Measured	Simulated
Sampling Frequency	50 MHz	50 MHz
Signal Bandwidth	8.33 MHz	8.33 MHz
SNDR (1.8 MHz)	40.3 dB	74.9 dB
SNR (1.8 MHz)	43.8 dB	N/A
SFDR (1.8 MHz)	48.3 dB	78.5 dB
Analog Power	135 mW	134 mW
Digital Power	16 mW	14 mW

Table 6.5: Summary of experimental results for the 8^{th}-order cascaded incremental A/D converter (simulated results do not include thermal noise).

6.5 Discussion

The experimental results of all three data converter modes can help explain the performance of the incremental data converter. The DC results for the pipeline A/D converter show discontinuities in the output code. These are characteristic of a gain error, but one where the gain is larger than 2. Gains that are smaller than 2 are typical when OTA DC gain is lower than required, or when capacitor mismatch is present. Low DC gain cannot account for gains that are larger than 2, and therefore it is assumed that capacitor mismatch is responsible for the larger gains.

The $\Delta\Sigma$ mode operates very well, similar to what is expected from simulations (aside from operating at a slower sampling frequency than the 100 MHz simulations, which is not surprising since the chip corner is slow). Both the pipeline and incremental modes do not operate as well, although the three architectures use identical circuitry aside from the clocking scheme. It is therefore assumed that the resetting clocks necessary for both the incremental and pipeline modes of operation are responsible for this deterioration in performance (these clocks are set in one position and do not toggle while the $\Delta\Sigma$ is operating).

The odd and even resetting clocks presented in Fig. 4.10 are maintained at either a high or low level while the $\Delta\Sigma$ is operating, but they are necessary for resetting the capacitors during the operation of both the pipeline and incremental modes. They are non-overlapping clocks with very tight restrictions on the non-overlap period since they fall within the non-overlap time of the regular two-phase clocking scheme (ϕ_1, ϕ_2). Simulations of the incremental data converter with parasitic capacitors do not account for the potential problems with these non-overlapping clocks. Long clock line metals on the chip which travel as much as 3 mm can add resistance to the clock lines that are not modeled. This causes the non-overlapping clock edges to slow to the point that they may potentially overlap and share charge with the other resetting capacitor in the circuit (for example, C_{2o} may share charge with C_{2e} in Fig. 4.10).

Fig. 6.17 shows a simulation of the operation of these clocks on the last stage of the data converter (about 2.5 mm from the clock generator) using the typical corner and adding parasitic line resistances in the clock lines along with parasitic capacitances. Also shown are unloaded clocks, and clocks with only parasitic capacitances modeled. It is clear that the line resistances significantly impact the clock rise and fall times. With R and C mod-

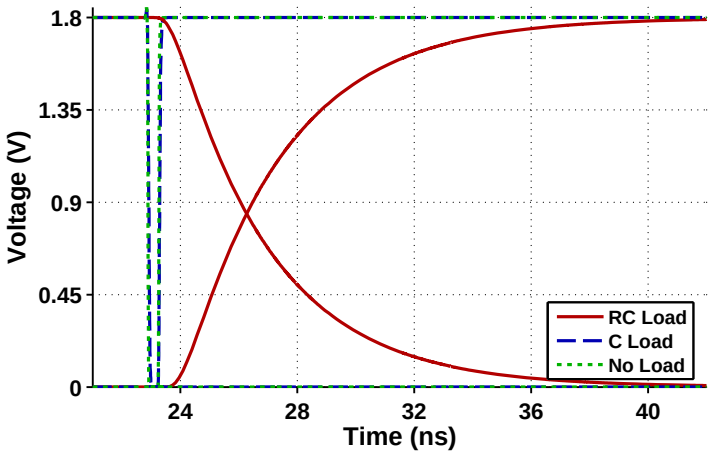


Figure 6.17: Non-overlapping resetting clocks in the presence of parasitic resistances and capacitances.

eled, the non-overlap time of about 320 ps disappears to the point that the clocks cross at 850 mV. This voltage is high enough to turn both switches on, causing the two integrating capacitors to share charge in both the pipeline and incremental modes of operation. Note that a decreased clock rate would not make a difference here because the non-overlap time of the clocks would still be the same.

System simulations were performed to evaluate the degradation in performance with the associated line resistances and capacitances. The SNDR of the incremental data converter degrades to 57.1 dB, and if the clock line impedances increase by 25 %, the SNDR degrades to 41.9 dB. These simulation results indicate that the additional clock line resistance is capable of degrading the performance to the extent observed in the experimental results. To correct these problems, the 1 µm wide clock lines should have been designed using wider metal widths to reduce this line resistance, and local inverters should have been used on the switches with stronger clock drivers. Also, a modified chip floorplan could help reduce the clock line length and resistance.

Chapter 7

Conclusions

This dissertation explored several methods of reducing the OSR of both incremental data converters and ΔΣ modulators. Typically ΔΣ modulators require high OSRs to reduce the in-band noise, but it was shown that a high-order cascaded ΔΣ can reduce the in-band noise sufficiently at an OSR as low as 3. Incremental data converters were also shown to attain higher SQNR at low OSRs when compared to similar ΔΣ modulators, and their extension to time-interleaved architectures was investigated. A prototype chip was designed in 0.18 µm CMOS technology and can operate in three modes by simply changing the clock phases. The prototype operates as an 8-stage pipeline A/D converter, an 8^{th}-order cascaded ΔΣ modulator, and an 8^{th}-order cascaded incremental data converter.

7.1 Summary

Chapter 1 introduced the topic and listed recent high-speed pipeline and ΔΣ data converters while Chapter 2 presented background information on a few relevant A/D converter architectures, focusing on the incremental data converter. Chapter 3 discussed the first contribution which was a low-OSR ΔΣ modulator. Chapter 4 presented the other two contributions, namely the low-OSR incremental A/D converter as well as the time-interleaved incremental data converter. The circuit design for the fabricated chip was described in detail in Chapter 5 while Chapter 6 presented the experimental results from the prototype chip in its three modes of operation as a pipeline A/D converter, a ΔΣ modulator and an incremental A/D converter. Chapter 7 concluded the dissertation. Appendix A and Appendix B

covered derivations of the incremental A/D converter resolution and the DC gain requirements, respectively. An alternative time-interleaved incremental data converter architecture was presented in Appendix C.

7.2 Contributions

Three main architectures were investigated for low OSR data conversion. The first was the cascaded high-order $\Delta\Sigma$ modulator which was experimentally shown to perform well, and has the potential to lower the power consumption of standard pipeline A/D converters at low OSRs. This work is the first to lower the OSR of $\Delta\Sigma$ modulators down to 3, and increase the number of cascaded stages to 8 [83].

The second contribution was the cascaded high-order incremental data converter. It was shown that incremental data converters possess SQNR advantages over $\Delta\Sigma$ modulators at low OSRs. These converters were analyzed with a removed input S/H, in the presence of DC gain errors, and with OSRs as low as 1 [70, 84], furthering the theoretical research into incremental data converters.

The final architecture investigated was the time-interleaved incremental data converter. Two potential architectures were identified, one of which required matching between parallel paths [51], and the other potentially overcoming this problem.

7.3 Future Directions

A few topics discussed throughout this dissertation were not thoroughly investigated and are worthy of future research.

7.3.1 Higher-Order Individual Stages

One topic is the use of higher-order individual stages in the cascaded architectures presented for both the incremental and $\Delta\Sigma$ modes of operation. If, for example, 2^{nd}-order modulators are used within the cascaded architecture, optimized zeros could further enhance the SQNR of the chosen architecture. These 2^{nd}-order individual stages would also reduce the stringent requirements on the DC gain of the analog circuitry since the error fed from the second stage rather than the first stage must be canceled.

7.3.2 Time-Interleaved Incremental Data Converters

The time-interleaved incremental architecture can be designed to overcome the attenuation that exists at higher input frequencies when the S/H is removed. While this architecture was not implemented, it would be worth investigating.

Another architecture that was not fully assessed was the unwound time-interleaved incremental A/D converter which was presented in Appendix C. Due to the elimination of the integrating/resetting amplifiers required in standard incremental operation, this architecture could be much easier to implement. It also avoids the matching problems inherent in the standard time-interleaved incremental architecture presented in Section 4.2.

7.3.3 Decimation Filter

Throughout this dissertation the incremental data converter was always assumed to use an L^{th}-order differentiator-type decimation filter for an L^{th}-order modulator. The disadvantage of using this decimation filter is the increased noise at low OSRs, as was shown in Table 2.1. However, there are alternative decimation filters which may be better suited to low-OSR design. These were mentioned briefly in Section 2.2.2 [46–48] and should be investigated as they may provide a solution for reducing the thermal noise at low OSRs.

7.3.4 OTA Power Down

One major difficulty with the incremental data converter was the resetting phase. At low OSRs it is more efficient to use fully-delaying stages to reduce the loading on the integrating/gain phase of the OTA, but the resulting resetting pulse must occur in the non-overlap time of the two-phase clocks. In pipeline A/D converters half-delaying stages can be efficient as long as the OTA can be powered down on the sampling phase to save the power that is otherwise lost on the loaded gain phase. Incremental data converters cannot take advantage of this savings since the OTA must remain powered to preserve the charge on the integrating capacitor. Finding a way to power down an OTA that is used as an integrator requires further research and could greatly reduce the clocking complexity of the incremental data converter.

7.3.5 Continuous-Time Cascaded Incremental Converters

A final topic worth investigating is the operation of cascaded incremental data converters using continuous-time rather than discrete-time circuits. Like dual-slope A/D converters, incremental data converters can be designed with continuous-time circuitry, but this has not been applied to cascaded architectures. Current research into continuous-time cascaded $\Delta\Sigma$ modulators [85, 86] indicates that the high-speed benefits of continuous-time circuitry can likely be applied to incremental data converters, but matching the time constants of the analog circuitry to the digital filters remains a challenge at high resolutions.

Appendices

Appendix A

Resolution of an Incremental A/D Converter

This appendix derives the number of output levels for an L^{th}-order incremental A/D converter with an NTF of $(1-z^{-1})^L$ at an OSR of M with an N-level quantizer, and a digital decimation filter equal to $(1-z^{-1})^L$. The A/D output $D_A[i]$ is assumed to be between ± 1 (i.e., $D_A[i] = \{-1, 1\}$ for $N = 2$, $D_A[i] = \{-1, 0, 1\}$ for $N = 3$, etc.), while the D/A output is the same value $D_A[i]$ multiplied by V_{REF}.

As a reference for the following derivations, an N-level quantizer with upper and lower quantizer levels ± 1 can have an input magnitude as large as $N/(N-1)$ without overloading the quantizer, meaning that the quantizer error magnitude is less than $1/(N-1)$. Input feedforward architectures are analyzed, and feedback architectures will yield the same number of output levels.

A.1 First-Order

Assuming a converter input where the quantizer input is not overloaded according to Eq. 2.16, the input to a binary quantizer is bounded by $-2V_{REF} < V_Q[M] < 2V_{REF}$ after M clock cycles where

$$V_Q[M] = \sum_{i=1}^{M} V_{IN}[i] - \sum_{i=1}^{M-1} V_{REF} \cdot D_A[i]. \tag{A.1}$$

Generalized to an N-level quantizer, the quantizer input will be bounded by

$$-\frac{N}{N-1} V_{REF} < V_Q[M] < \frac{N}{N-1} V_{REF}. \tag{A.2}$$

The last digital output $V_{REF} \cdot D_A[M]$ is the N-level quantized value of the input $V_Q[M]$. As long as the inequality of Eq. A.2 holds, the difference between the input $V_Q[M]$ and the output $V_{REF} \cdot D_A[M]$ must be constrained by the inequality

$$-\frac{1}{N-1}V_{REF} < V_Q[M] - V_{REF} \cdot D_A[M] < \frac{1}{N-1}V_{REF} \tag{A.3}$$

or equivalently,

$$\begin{aligned}\frac{1}{N-1}V_{REF} &> \Big|V_Q[M] - V_{REF} \cdot D_A[M]\Big| \\ &= \Big|\sum_{i=1}^{M} V_{IN}[i] - \sum_{i=1}^{M-1} V_{REF} \cdot D_A[i] - V_{REF} \cdot D_A[M]\Big| \\ &= \Big|MV_{IN} - \sum_{i=1}^{M} V_{REF} \cdot D_A[i]\Big|. \end{aligned} \tag{A.4}$$

Dividing both sides by M and V_{REF}, the resulting inequality is

$$\frac{1}{M(N-1)} > \Big|\frac{V_{IN}}{V_{REF}} - \frac{1}{M}\sum_{i=1}^{M} D_A[i]\Big|. \tag{A.5}$$

The digital output of the incremental A/D converter, scaled for digital values between ± 1, is $\frac{1}{M}\sum_{i=1}^{M} D_A[i]$. Therefore, the inequality of Eq. A.5 defines the error between the digital output of the incremental A/D converter and the normalized input V_{IN}/V_{REF}. Since the error magnitude is less than $1/M(N-1)$, and the error is uniformly distributed according to Eq. A.5 (as expected in the staircase outputs shown in Fig. 2.8 and Fig. 2.10 and verified in simulation), the A/D converter has $M(N-1)+1$ output levels.

A.2 Second-Order Single-Stage

Analyzing the 2nd-order input feed-forward modulator of Fig. 2.9, the first integrator output is

$$\begin{aligned} V_{I,1}[1] &= 0 \\ V_{I,1}[2] &= V_{IN}[1] - V_{REF} \cdot D_A[1] \\ V_{I,1}[3] &= V_{IN}[1] + V_{IN}[2] - V_{REF} \cdot (D_A[1] + D_A[2]) \end{aligned}$$

$$\vdots$$

$$V_{I,1}[M] = \sum_{i=1}^{M-1} (V_{IN}[i] - V_{REF} \cdot D_A[i]). \tag{A.6}$$

The second integrator output is

$$\begin{aligned}
V_{I,2}[1] &= 0 \\
V_{I,2}[2] &= V_{I,1}[1] = 0 \\
V_{I,2}[3] &= V_{I,1}[2] + V_{I,1}[1] = V_{IN}[1] - V_{REF} \cdot D_A[1] \\
V_{I,2}[4] &= V_{I,1}[3] + V_{I,1}[2] + V_{I,1}[1] \\
&= 2V_{IN}[1] + V_{IN}[2] - V_{REF} \cdot (2D_A[1] + D_A[2]) \\
&\vdots \\
V_{I,2}[M] &= \sum_{i=2}^{M-1} V_{I,1}[i] \\
&= \sum_{i=2}^{M-1} \sum_{j=1}^{i-1} (V_{IN}[j] - V_{REF} \cdot D_A[j]).
\end{aligned} \tag{A.7}$$

The input to the quantizer is

$$\begin{aligned}
V_Q[M] =& V_{I,2}[M] + 2V_{I,1}[M] + V_{IN}[M] \\
&= \sum_{i=2}^{M-1} \sum_{j=1}^{i-1} (V_{IN}[j] - V_{REF} \cdot D_A[j]) \\
&\quad + 2 \sum_{i=1}^{M-1} (V_{IN}[i] - V_{REF} \cdot D_A[i]) + V_{IN}[M].
\end{aligned} \tag{A.8}$$

Assuming V_{IN} keeps the quantizer input from overloading, the input to the quantizer is again bounded according to

$$\frac{N}{N-1} V_{REF} > \left| V_Q[M] \right|. \tag{A.9}$$

Adding the last digital output $V_{REF} \cdot D_A[M]$, the resulting inequality (with some rearranging of Eq. A.8) is

$$\frac{1}{N-1} V_{REF} > \left| V_Q[M] - V_{REF} \cdot D_A[M] \right|$$

$$= \left| \sum_{i=1}^{M} \sum_{j=1}^{i} (V_{IN}[j] - V_{REF} \cdot D_A[j]) \right|$$
$$= \left| \frac{M(M+1)}{2} V_{IN} - \sum_{i=1}^{M} \sum_{j=1}^{i} V_{REF} \cdot D_A[j]) \right| \quad \text{(A.10)}$$

Dividing both sides by $M(M+1)/2$ and V_{REF}, the inequality becomes

$$\frac{2}{M(M+1)(N-1)} > \left| \frac{V_{IN}}{V_{REF}} - \frac{2}{M(M+1)} \sum_{i=1}^{M} \sum_{j=1}^{i} D_A[i] \right|. \quad \text{(A.11)}$$

The scaled digital output D_{OUT} of the 2nd-order incremental A/D converter is

$$\frac{2}{M(M+1)} \sum_{i=1}^{M} \sum_{j=1}^{i} D_A[i]. \quad \text{(A.12)}$$

Therefore, the inequality again defines the error between the digital output of the incremental converter and the normalized input. The error is less than $2/M(M+1)(N-1)$, so the A/D converter has $M(M+1)(N-1)/2+1$ output levels.

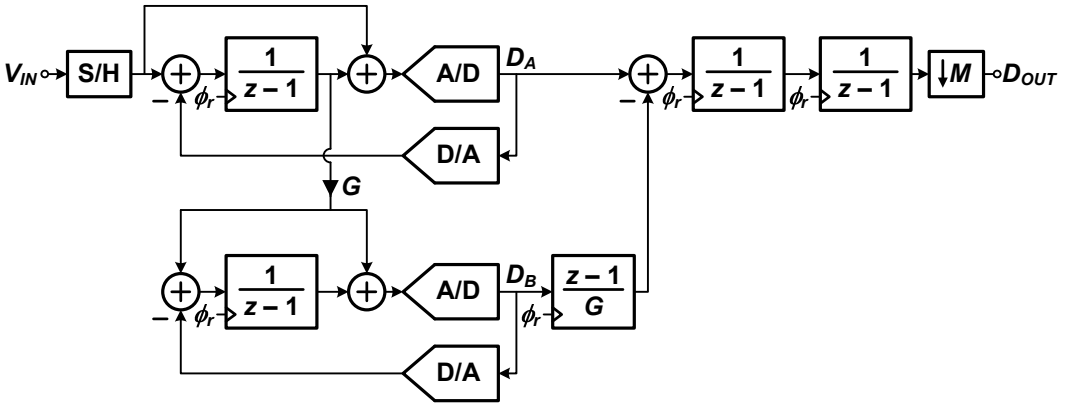


Figure A.1: A 2nd-order input feed-forward cascaded incremental A/D converter.

A.3 Second-Order Cascaded

To analyze a 2nd-order cascaded architecture, the input feed-forward modulator of Fig. A.1 will be used. The first quantizer has N_1 levels while the second quantizer has N_2 levels. The

first integrator output is

$$\begin{aligned}
V_{I,1}[1] &= 0 \\
V_{I,1}[2] &= V_{IN}[1] - V_{REF} \cdot D_A[1] \\
V_{I,1}[3] &= V_{IN}[1] + V_{IN}[2] - V_{REF} \cdot (D_A[1] + D_A[2]) \\
&\vdots \\
V_{I,1}[M+1] &= \sum_{i=1}^{M} (V_{IN}[i] - V_{REF} \cdot D_A[i]).
\end{aligned} \tag{A.13}$$

$M+1$ samples are taken since there is a delay from the input to the second stage. The integrator output gets multiplied by the gain G and becomes the input to the second integrator. The input to the second quantizer becomes

$$\begin{aligned}
V_{Q,2}[1] =& 0 \\
V_{Q,2}[2] =& GV_{I,1}[2] = GV_{IN}[1] - GV_{REF} \cdot D_A[1] \\
V_{Q,2}[3] =& GV_{I,1}[3] + GV_{I,1}[2] - V_{REF} \cdot D_B[2] \\
=& 2GV_{IN}[1] + GV_{IN}[2] - GV_{REF} \cdot (2D_A[1] + D_A[2]) \\
& - V_{REF} \cdot D_B[2] \\
&\vdots \\
V_{Q,2}[M+1] =& G \sum_{i=2}^{M+1} \sum_{j=1}^{i-1} (V_{IN}[j] - V_{REF} \cdot D_A[j]) \\
& - \sum_{i=2}^{M} V_{REF} \cdot D_B[i].
\end{aligned} \tag{A.14}$$

Assuming that V_{IN} keeps the quantizer input from overloading, and that the gain factor G increases the error term from the previous stage such that the input to the second stage also keeps the second quantizer input from overloading, then the input to the second quantizer is bounded according to

$$\frac{N_2}{N_2 - 1} V_{REF} > \Big| V_{Q,2}[M+1] \Big|. \tag{A.15}$$

Adding the last digital output $V_{REF} \cdot D_B[M+1]$, the resulting inequality is

$$\begin{aligned}\frac{1}{N_2-1}V_{REF} &> \Big|V_Q[M+1] - V_{REF}\cdot D_B[M+1]\Big| \\ &= \Big|G\sum_{i=2}^{M+1}\sum_{j=1}^{i-1}(V_{IN}[j] - V_{REF}\cdot D_A[j]) \\ &\quad - \sum_{i=2}^{M} V_{REF}\cdot D_B[i] - V_{REF}\cdot D_B[M+1]\Big| \\ &= \Big|G\frac{M(M+1)}{2}V_{IN} - G\sum_{i=2}^{M+1}\sum_{j=1}^{i-1}V_{REF}\cdot D_A[j] \\ &\quad - \sum_{i=2}^{M+1} V_{REF}\cdot D_B[i]\Big|. \end{aligned} \tag{A.16}$$

Dividing both sides by $GM(M+1)/2$ and V_{REF}, the inequality becomes

$$\begin{aligned}\frac{2}{GM(M+1)(N_2-1)} > \Big|&\frac{V_{IN}}{V_{REF}} - \frac{2}{M(M+1)}\sum_{i=1}^{M}\sum_{j=1}^{i} D_A[j] \\ &- \frac{2}{M(M+1)}\sum_{i=2}^{M+1}\frac{D_B[i]}{G}\Big|. \end{aligned} \tag{A.17}$$

Referring to Fig. A.1, the digital output D_{OUT} of the 2nd-order cascaded incremental A/D converter is

$$\sum_{i=1}^{M}\sum_{j=1}^{i} D_A[j] + \frac{1}{G}\sum_{i=2}^{M+1}\sum_{j=2}^{i}(D_B[j] - D_B[j-1]). \tag{A.18}$$

Since $D_B[1] = 0$ (no input has affected the second stage after one sample), the resulting digital output is

$$\sum_{i=1}^{M}\sum_{j=1}^{i} D_A[j] + \sum_{i=2}^{M+1}\frac{D_B[i]}{G}. \tag{A.19}$$

This digital output is identical to the digital signal subtracted from the normalized input signal in the inequality of Eq. A.17 (aside from the scaling factor of $2/M(M+1)$ which keeps the digital signal between ± 1).

The inequality of Eq. A.17 defines the error between the digital output of the cascaded incremental converter and the normalized input, and the error is less than $2/GM(M+1)(N_2-1)$ so the A/D converter has $GM(M+1)(N_2-1)/2+1$ output levels. Since the

first quantizer has N_1-levels, if a converter input of unity keeps the second stage quantizer bounded (as is the case for this particular example), G can be as large as $N_1 - 1$, and the resulting number of output levels is

$$\frac{(N_1-1)(N_2-1)M(M+1)}{2}+1. \tag{A.20}$$

A.4 Extension to Higher-Order

For single-stage architectures, the results can be generalized to higher-order converters, and the number of output levels is

$$(N-1)\frac{(M+L-1)!}{L!(M-1)!}+1. \tag{A.21}$$

It can be seen that this equation works for previous cases, and it should be clear how the previous analysis can be extended to 3$^{\text{rd}}$-order, 4$^{\text{th}}$-order, and higher order converters (although it becomes quite tedious).

For cascaded architectures the results can also be generalized to higher-order converters. The equation is similar to that for the single-stage architecture, except that the number of output levels is increased (roughly) by the gain factor G_i associated with each stage. The resulting number of output levels for n stages is

$$(N_n-1)\prod_{i=1}^{n-1} G_i \frac{(M+L-1)!}{L!(M-1)!}+1. \tag{A.22}$$

If the stages are all identical 1$^{\text{st}}$-order stages where a full-scale input keeps the quantizers bounded, then assuming each stage quantizer has N-levels, and $G = N-1$, the resulting equation is

$$(N-1)^L\frac{(M+L-1)!}{L!(M-1)!}+1. \tag{A.23}$$

For an 8$^{\text{th}}$-order cascaded incremental A/D converter with 1$^{\text{st}}$-order 3-level quantizer stages, the number of output levels is

$$2^8\frac{(M+7)!}{8!(M-1)!}+1 \tag{A.24}$$

as the OSR M is varied. This is how the SQNR for the incremental A/D converter in Fig. 4.1 is found. It was also verified with simulations and matched the predicted resolution.

Appendix B

Finite DC Gain in Incremental A/D Converters

Section 4.2.3 illustrated the required back-end filter in the presence of finite DC gain (and capacitor mismatch) errors. Without this filter the converter may still resolve to a sufficient resolution as long as the DC gain is high enough. This appendix derives the DC gain requirements of an uncalibrated incremental A/D converter. The analysis focuses on an OSR of 3, but could be extended to different OSRs if necessary.

B.1 DC Gain Requirements

Deriving the DC gain requirements is more involved with an incremental A/D converter than with a $\Delta\Sigma$ modulator. Similar to a $\Delta\Sigma$ model, an integrator can be assumed to have a transfer function

$$I(z) = \frac{C_1}{C_2}\frac{a}{z-p} \tag{B.1}$$

where a and p are defined as in Eq. 4.12 and Eq. 4.13 where

$$a = \frac{1}{1+(1+C_1/C_2)/A} \tag{B.2}$$

$$p = \frac{1+1/A}{1+(1+C_1/C_2)/A}. \tag{B.3}$$

The important difference for the analysis is that this integrator operates as a gain stage in the first clock cycle before it starts integrating. Analyzing the time-domain behaviour of the incremental converter for 3 time steps (at an OSR of 3), the downsampled digital output

of a 1st-order converter is

$$\begin{aligned} D_{OUT} \cdot V_{REF} =& V_{IN}[1] + V_{IN}[2] + V_{IN}[3] \\ &+ E_1[3] + (1-a_1)E_1[2] + (1-a_1+a_1(a_1-p_1))E_1[1] \end{aligned} \tag{B.4}$$

where $V_{IN}[i]$ is the input, $E_n[i]$ is the quantizer noise at the i^{th} time instant from the n^{th} stage, and a_n and p_n are the constants used to model the n^{th} stage integrator.

If the same analysis is performed for a 2nd-order converter, the downsampled digital output is

$$\begin{aligned} D_{OUT} =& 3V_{IN}[1] + 2V_{IN}[2] + V_{IN}[3] \\ &+ (3(1-a_1) + 2a_1(a_1-p_1) - a_1(a_1-p_1)^2)E_1[1] \\ &+ (2(1-a_1) + a_1(a_1-p_1))E_1[2] \\ &+ (1-a_1)E_1[3] \\ &+ ((1-a_2) + a_2(a_2-p_2))E_2[1]/2 \\ &+ (1-a_2))E_2[2]/2 \\ &+ E_2[3]/2. \end{aligned} \tag{B.5}$$

The equations have been grouped to help illustrate the contributions from each quantizer. If the DC gain is infinite, the a_i and p_i terms are unity and only the first and last lines would remain (as expected from Section 4.3.2).

Extending this analysis to an 8th-order converter, the downsampled digital output is

$$\begin{aligned} D_{OUT} =& 36V_{IN}[1] + 8V_{IN}[2] + V_{IN}[3] \\ &+ (36(1-a_1) + 8a_1(a_1-p_1) - a_1(a_1-p_1)^2)E_1[1] \\ &+ (8(1-a_1) + a_1(a_1-p_1))E_1[2] \\ &+ (1-a_1)E_1[3] \\ &+ (28(1-a_2) + 7a_2(a_2-p_2) - a_2(a_2-p_2)^2)E_2[1]/2 \\ &+ (7(1-a_2) + a_2(a_2-p_2))E_2[2]/2 \\ &+ (1-a_2)E_2[3]/2 \\ &+ (21(1-a_3) + 6a_3(a_3-p_3) - a_3(a_3-p_3)^2)E_3[1]/4 \end{aligned}$$

$$
\begin{aligned}
&+(6(1-a_3)+a_3(a_3-p_3))E_3[2]/4\\
&+(1-a_3)E_3[3]/4\\
&+(15(1-a_4)+5a_4(a_4-p_4)-a_4(a_4-p_4)^2)E_4[1]/8\\
&+(5(1-a_4)+a_4(a_4-p_4))E_4[2]/8\\
&+(1-a_4)E_4[3]/8\\
&+(10(1-a_5)+4a_5(a_5-p_5)-a_5(a_5-p_5)^2)E_5[1]/16\\
&+(4(1-a_5)+a_5(a_5-p_5))E_5[2]/16\\
&+(1-a_5)E_5[3]/16\\
&+(6(1-a_6)+3a_6(a_6-p_6)-a_6(a_6-p_6)^2)E_6[1]/32\\
&+(3(1-a_6)+a_6(a_6-p_6))E_6[2]/32\\
&+(1-a_6)E_6[3]/32\\
&+(3(1-a_7)+2a_7(a_7-p_7)-a_7(a_7-p_7)^2)E_7[1]/64\\
&+(2(1-a_7)+a_7(a_7-p_7))E_7[2]/64\\
&+(1-a_7)E_7[3]/64\\
&+((1-a_8)+a_8(a_8-p_8))E_8[1]/128\\
&+(1-a_8))E_8[2]/128\\
&+E_8[3]/128. \qquad \text{(B.6)}
\end{aligned}
$$

If the finite DC gain from only the first stage is considered, the resulting output is

$$
\begin{aligned}
D_{OUT} =&36V_{IN}[1]+8V_{IN}[2]+V_{IN}[3]\\
&+(36(1-a_1)+8a_1(a_1-p_1)-a_1(a_1-p_1)^2)E_1[1]\\
&+(8(1-a_1)+a_1(a_1-p_1))E_1[2]\\
&+(1-a_1)E_1[3]\\
&+E_8[3]/128. \qquad \text{(B.7)}
\end{aligned}
$$

Substituting the values of a_i and p_i with $C_1/C_2 = 2$, assuming the error signals are uncorrelated, and keeping in mind that the error signals are half the size of a full-scale input since they are generated with a 3-level quantizer, the error signal will be approximately (within

10 %) A times less than the input. For an incremental A/D converter with N-bit resolution limited by finite DC gain, $A \approx 2^N$.

Appendix C

Unwinding the Incremental

Section 4.2 discussed an approach to time-interleaved incremental data converters that requires matching between the different time-interleaved paths. This appendix presents another architecture that acquires the same transfer function in a time-interleaved manner with only a single path.

C.1 Time-Interleaved Algorithmic Data Converters

An algorithmic or cyclic data converter [45] is similar to a single stage of a pipeline data converter. Shown in Fig. C.1, the input is held and quantized with a low-resolution comparator, then the difference between the input and the digital output is amplified and fed back to the input where this procedure is repeated. The converter resolution is increased as the number of feedback cycles are increased.

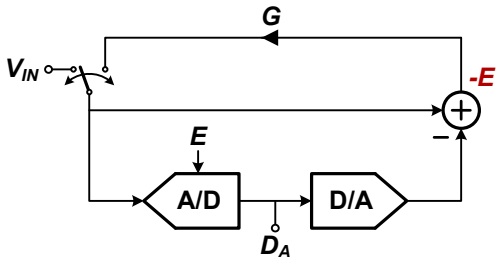


Figure C.1: Algorithmic data converter.

The digital output of an algorithmic data converter is based solely on the signal that appears at the input to the low-resolution comparator at each quantizing instant. The input to the quantizer after one period is

$$V_Q[1] = V_{IN}[1] \tag{C.1}$$

and the output is $V_{REF} \cdot D_A[1]$ (the digital output is $D_A[1]$ while the analog output is the digital output multiplied by V_{REF}). After two periods the input to the quantizer is

$$V_Q[2] = G(V_{IN}[1] - V_{REF} \cdot D_A[1]) \tag{C.2}$$

and after M periods the input to the quantizer is

$$\begin{aligned} V_Q[M] = G^{M-1}V_{IN}[1] - G^{M-1}V_{REF} \cdot D_A[1] - G^{M-2}V_{REF} \cdot D_A[2] - \ldots \\ - G^1 V_{REF} \cdot D_A[M-1]. \end{aligned} \tag{C.3}$$

This can be compared to the sequence of pipeline quantizer inputs of Fig. 2.12 for the n^{th} stage

$$V_Q[n] = V_{IN}\prod_{i=1}^{n-1} G_i - V_{REF} \cdot D_1 \prod_{i=1}^{n-1} G_i - V_{REF} \cdot D_2 \prod_{i=1}^{n-2} G_i - \ldots - D_{n-1} \cdot V_{REF} \cdot G_1. \tag{C.4}$$

If n is equated to the period M and the gains

$$G = G_1 = G_2 = \ldots = G_n \tag{C.5}$$

then the two equations are identical and the output of the algorithmic A/D converter is identical to that of a pipeline converter. The difference is that the algorithmic converter takes M cycles to resolve one input while the pipeline data converter (as the name implies) pipelines the decisions and is able to operate on M times as many inputs.

If the pipeline input is held for M periods, the pipeline data converter is effectively an oversampled algorithmic data converter. When the input is not held, it is effectively a time-interleaved algorithmic converter. An algorithmic data converter is conceptually wound up in the signal loops around the converter, and by unwinding it the signal passes straight

through, increases the throughput, and becomes a pipeline A/D converter.

C.2 Time-Interleaved Incremental Data Converters

In the same way that an algorithmic data converter can be unwound into a pipeline data converter, an incremental data converter can be unwound into a time-interleaved incremental data converter. As in the previous section, the architecture of Fig. 2.8 can be converted to a time-interleaved equivalent, as long as the inputs of the low-resolution quantizer remain constant.

The input to the quantizer after one period is

$$V_Q[1] = V_{IN}[1] \tag{C.6}$$

and the input to the quantizer after M periods is

$$V_Q[M] = \sum_{i=1}^{M} V_{IN}[i] - \sum_{i=1}^{M-1} V_{REF} \cdot D_A[i]. \tag{C.7}$$

An unwound, time-interleaved equivalent of a 1$^{\text{st}}$-order incremental data converter is shown in Fig. C.2 which generates the transfer function of Eq. C.7 for $M = 3$. The quantizer inputs are (assuming the S/H is removed)

$$\begin{aligned} V_Q[1] &= V_{IN}[1] \\ V_Q[2] &= V_{IN}[1] + V_{IN}[2] - V_{REF} \cdot D_A[1] \\ V_Q[3] &= V_{IN}[1] + V_{IN}[2] + V_{IN}[3] - V_{REF}(D_A[1] + D_A[2]). \end{aligned} \tag{C.8}$$

When compared to the time-interleaved structure of Section 4.2, this architecture only uses gain stages to sum and delay signals and does not require resettable integrators (which were found to be problematic in the design), and it should consume less power because only $M-1$ delay stages are necessary for a time-interleaved by M architecture (the time-interleaved architecture of Fig. 4.11 effectively requires M stages). Another advantage of the unwound incremental architecture is that only a single path exists. Mismatch between time-interleaved stages is not a problem as every signal passes through the same circuits.

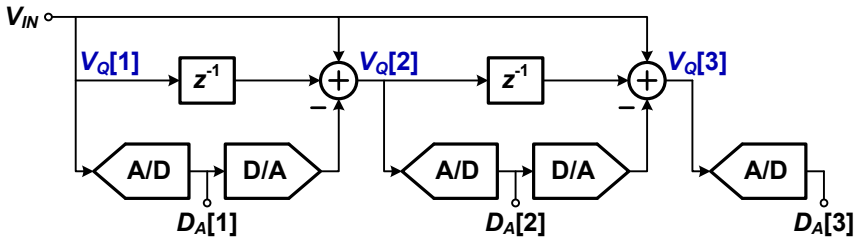


Figure C.2: Time-interleaved 1st-order incremental data converter derived from an unwound incremental data converter.

To extend the example to a higher-order architecture, the quantizer inputs for a 2nd-order incremental data converter with $M = 3$ are

$$\begin{aligned} V_Q[1] &= V_{IN}[1] \\ V_Q[2] &= 2V_{IN}[1] + V_{IN}[2] - 2V_{REF} \cdot D_A[1] \\ V_Q[3] &= 3V_{IN}[1] + 2V_{IN}[2] + V_{IN}[3] - 3V_{REF} \cdot D_A[1] - 2V_{REF} \cdot D_A[2]. \end{aligned} \tag{C.9}$$

The equivalent architecture is shown in Fig. C.3. The architecture starts getting more complicated as the order is increased since more inputs to each stage are necessary from preceding stages.

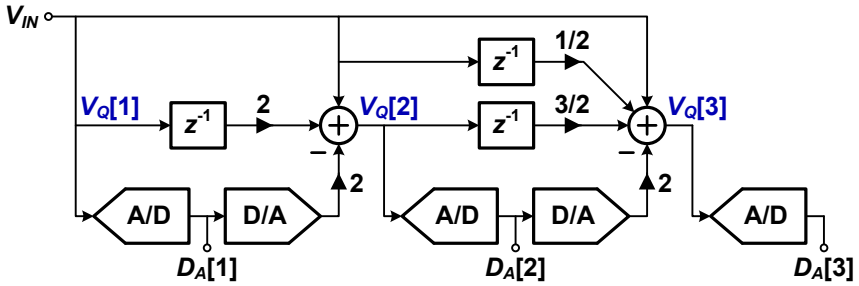


Figure C.3: Time-interleaved 2nd-order incremental data converter derived from an unwound incremental data converter.

The same analysis can also be applied to cascaded structures. For an n-stage cascaded incremental data converter, about n times as much circuitry is required. As an example, a 1-1 cascaded incremental with $M = 3$ is shown in Fig. C.4. The inputs to the first quantizer are the same as those for the 1st-order unwound incremental converter in Eq. C.8. The

inputs to the second quantizer are

$$\begin{aligned}
V_{Q2}[1] =& 0 \\
V_{Q2}[2] =& GV_{IN}[1] - GV_{REF} \cdot D_A[1] \\
V_{Q2}[3] =& 2GV_{IN}[1] + GV_{IN}[2] - GV_{REF} \cdot (2D_A[1] + D_A[2]) - V_{REF} \cdot D_B[2] \\
V_{Q2}[4] =& 3GV_{IN}[1] + 2GV_{IN}[2] + GV_{IN}[1] - GV_{REF} \cdot (3D_A[1] + 2D_A[2] + D_A[1]) \\
& - V_{REF} \cdot (D_B[2] + D_B[3]).
\end{aligned} \tag{C.10}$$

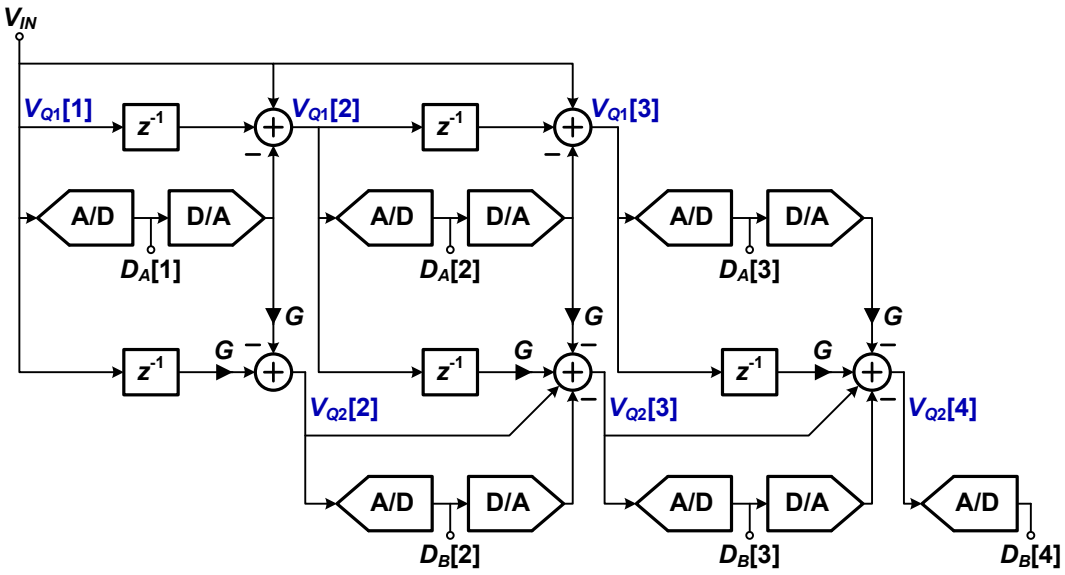


Figure C.4: Time-interleaved 1-1 cascaded 2nd-order incremental data converter.

The unwound incremental data converter has several advantages over the standard time-interleaved incremental architecture. Resetting every M clock cycles is unnecessary, and matching between parallel paths is no longer a problem. Further investigation into its robustness in the presence of circuit non-idealities is necessary to assess the practicality of this architecture.

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